## Module - I

BJT Biasing : Application of DC voltages to a transistor establishes a fixed level of current and voltage which establishes an operating point on the output characteristics.

Since the operating point is a fixed point on the characteristic it is called Quiescent point i.e Q-point for proper amplification.

Q-point is fixed in the middle of the active region.

The transistor can be biased in active or linear region based on the following conditions.

The Base-Emitter Junction should be forward biased & collector Emitter should be reverse biased

Transistor region of operation.

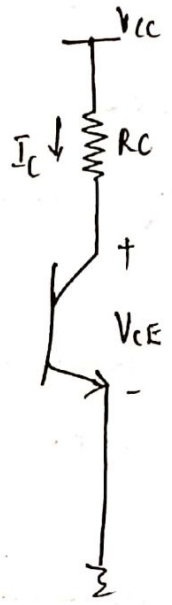
Active Region : B-E Junction is forward bias and C-E Junction reverse bias.

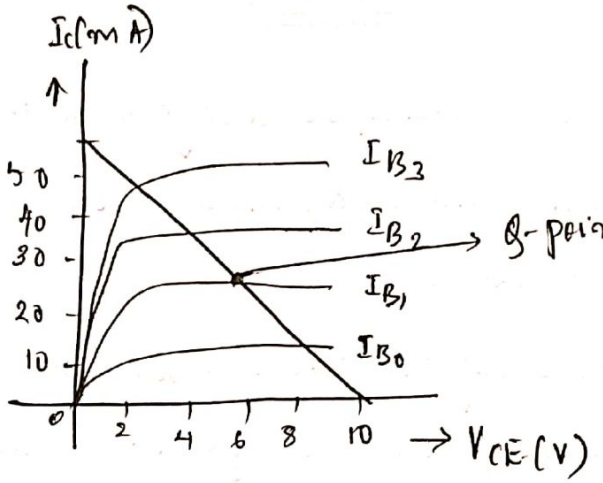
Saturation Region : B-E Junction is forward bias and C-E Junction forward bias.

Cut-off Region : B-E Junction is Reverse biased & C-E Junction reverse bias.

Operating point or DC load line : The line called dc load line can be drawn on the characteristic of the transistor which represents the applied load. The intersection of the load line with characteristics will determine the operating point

Consider C-E Circuit as shown below & Apply KVL to Ckt




Biased transistor along with the characteristics with dc load line analysis:

Apply KVL to C-E $\Rightarrow$ $V_{CC} - I_C R_C - V_{CE} = 0$

$$V_{CC} = I_C R_C + V_{CE} \rightarrow (1)$$

The $V_{CE}$ axis intercept can be found by choosing $I_C = 0$, in Eqn (1)

$$\boxed{V_{CC} = V_{CE}}$$

The $I_C$ axis intercept can be found by choosing $V_{CE} = 0$ in Eqn (1)

$$\boxed{I_C = V_{CC}/R_C}$$

Equation for the dc load line in the slope intercept from Eqn (1)

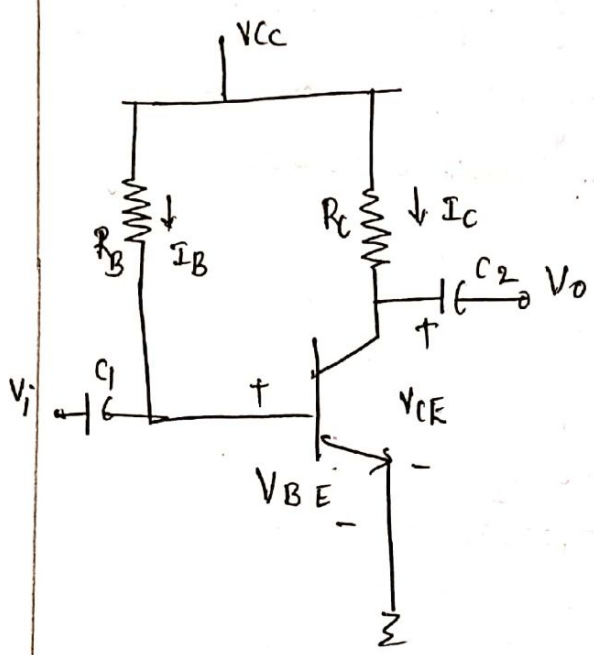
$$\boxed{I_C = (-1/R_C) V_{CE} + V_{CC}/R_C}$$

where the slope is $-1/R_C$ while the intercept is $V_{CC}/R_C$. The intersection of this load line with the output characteristics results in possible operating points. The operating point is chosen around the middle of the load line to provide an equal swing of $I_C$ and $V_{CE}$ about the point.

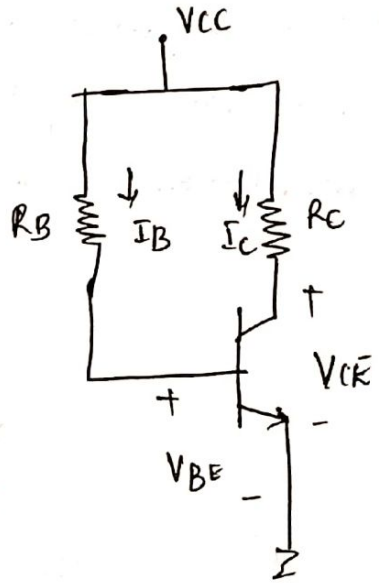
## Types of Biasing

1. Fixed bias or Base bias ckt
2. Emitter bias or Emitter stabilized biasing
3. Voltage divider / current gain stabilized or $\beta$ independent / universal bias
4. DC bias with feedback.

Fixed bias : Consider the ckt shown below neglect $C_1$ & $C_2$ for DC analysis




Fixed bias ckt with capacitor




DC bias

Apply KVL to Base to Emitter loop we get

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \rightarrow (1)$$

$$\boxed{I_C = \beta I_B} \rightarrow \text{Collector Current.}$$

Since the supply voltage $V_{CC}$ and $V_{BE}$ are constant once the resistance $R_B$ is selected $I_B$ is also fixed. Hence the circuit is called fixed bias ckt

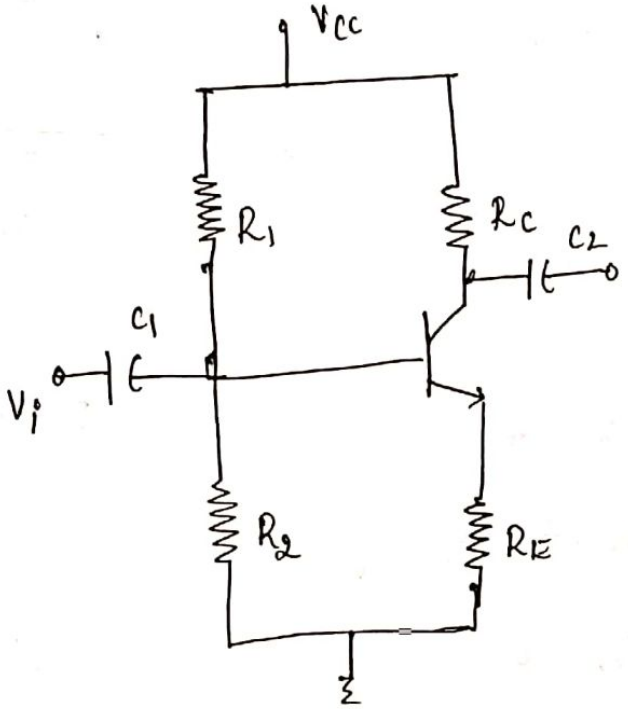
Apply KVL to C-E loop

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \rightarrow (3).$$

For fixed bias CKt $V_{BE} = V_B$, $V_E = 0$

Voltage Divider Bias : In the fixed bias and Emitter bias circuit the quiescent values of $I_C$ & $V_{CE}$ i.e Q-points is a function of dc currents gain $\beta$ of the transistor. W.K.T this current gain $\beta$ is sensitive to temperature and its values keep varying. A Biasing ckt independent or less independent on $\beta$ such as Voltage divider circuit is desirable




Vtg divider bias or universal bias ckt.

The voltage divider bias circuit can be analyzed in two methods.

→ Exact Method

→ Approximate method.

Exact Analysis : The input side of the CKt i.e B-E CKt of the figure is redrawn as shown in the figure below for dc analysis.

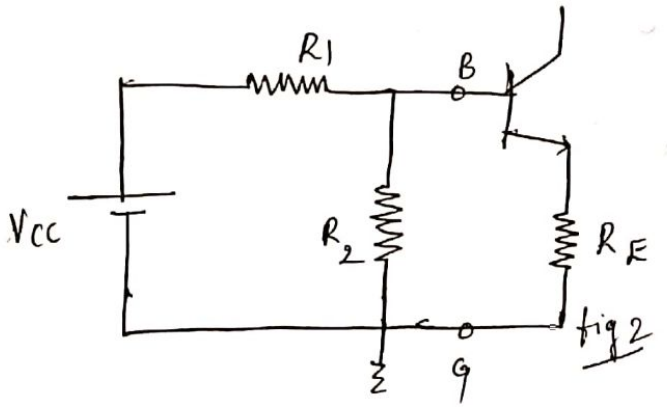
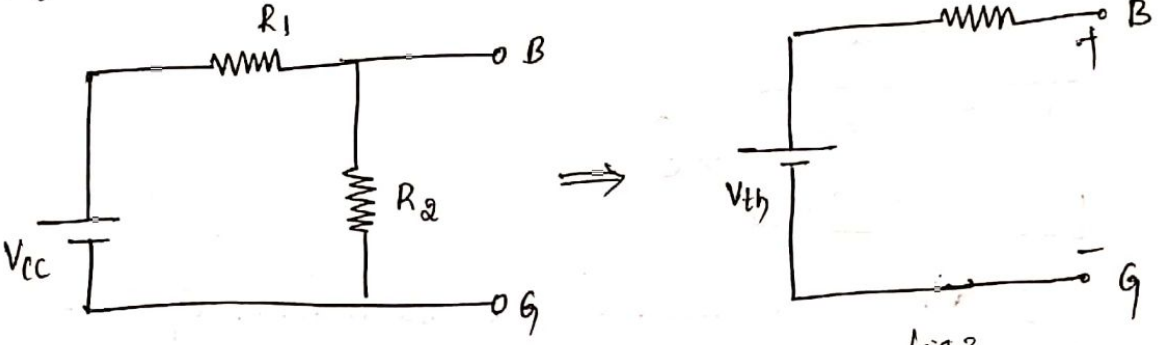



fig 2

The thevnin Equivalent of the CKt comprising of Vcc, $R_1$ & $R_2$ of the above figure shown below.




Thevnin Equivalent

fig 3

To find Rth i.e thevenin resistance Rth, Vcc is reduced to Zero in the above CKt.

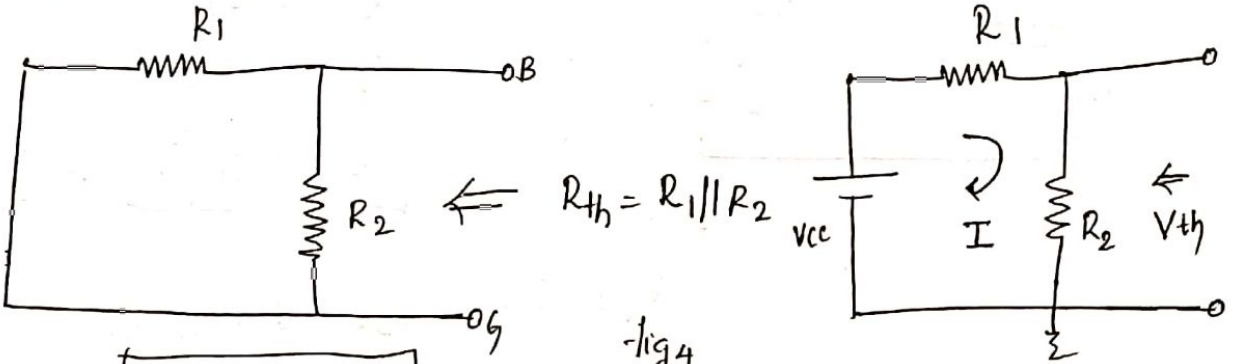



fig 4

Determination of Rth

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2} \rightarrow (1)$$

Determination of Vth

Apply KVL to I/p loop we get

$$V_{cc} - IR_1 - IR_2 = 0$$

$$V_{cc} - I(R_1 + R_2) = 0$$

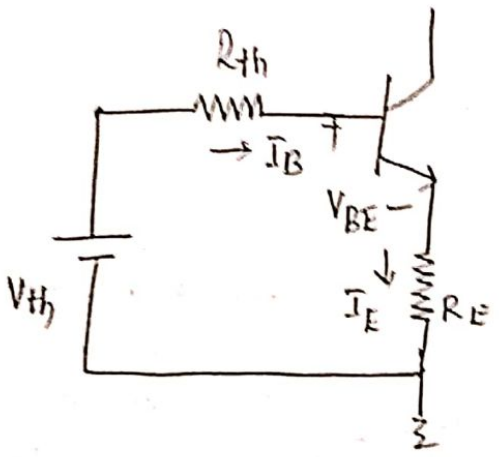
$$\boxed{I = \frac{V_{cc}}{R_1 + R_2}}$$

Voltage drop across $R_2$ is

$$V_{th} = I R_2$$

$$\boxed{V_{th} = \frac{V_{cc} R_2}{R_1 + R_2}} \rightarrow (2).$$

The fig (2) ckt is redrawn below to the Thevenin equivalent b/w B & E




Apply KVL to B-E loop.

$$V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

$$I_E = I_C + I_B$$

$$I_E = \beta I_B + I_B$$

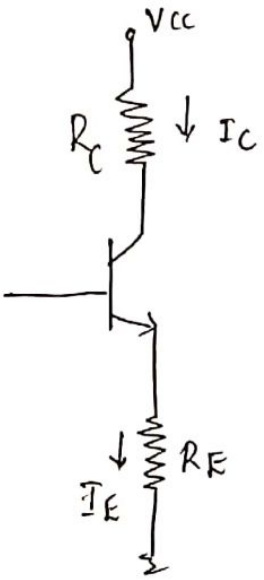
$$\boxed{I_E = I_B(1+\beta)} \rightarrow (3)$$

$$V_{th} = I_B R_{th} + V_{BE} + I_B(1+\beta) R_E$$

$$V_{th} = I_B (R_{th} + (1+\beta) R_E + V_{BE}$$

$$\boxed{I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1+\beta) R_E}} \rightarrow (4)$$

Consider C-E ckt




Applying KVL to ckt

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

WKT $I_E \simeq I_C$

$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0$$

$$V_{CC} - I_C (R_C + R_E) - V_{CE} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$

$V_E$ = Voltage across $R_E$

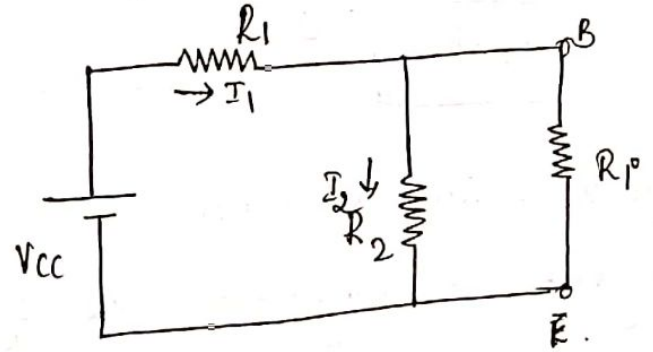
$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E$$

$$V_B = V_{BE} + V_E$$

In this circuit negative feedback is provided through the Emitter resistance As a result $I_C$ & $V_{CE}$ become almost independent of $\beta$. For this reason Voltage divider bias is also called as <u>beta-independent ckt</u>.

<u>Approximate analysis</u>: The resistance $R_E$ in the Emitter ckt gets reflected as $(1+\beta) R_E$ in the base ckt. Therefore the ckt b/w base & ground in figure can be replaced by an equivalent resistance $R_1' = (1+\beta) R_E$.




Input Circuit for Approximate analysis.

For the CKt given above using KCL we get.

$$I_1 = I_2 + I_B \rightarrow (1)$$

$R_i' = (1+\beta) R_E$ Since $\beta \gg 1$

$$\boxed{R_i' = \beta R_E} \rightarrow (4)$$

$I_B = V_B/R_1 \qquad I_2 = V_B/R_2$

$$\boxed{R_i' = \beta R_E \geq 10 R_2} \rightarrow (2)$$

Then $I_B \leq 0.1 I_2$, Hence $I_B$ can be neglected in Eq (1)

$$I_1 = I_2$$

Apply KVL to CKt

$$V_{CC} = I_1 R_1 + I_2 R_2$$

$$V_{CC} = I_2 (R_1 + R_2)$$

$$\boxed{I_2 = \frac{V_{CC}}{R_1 + R_2}}$$

Drop across $R_2$ i.e $V_B = I_2 R_2$

$$\boxed{V_B = \frac{V_{CC} R_2}{R_1 + R_2}} \rightarrow (3)$$

Observe the expression for $V_B$ is identical to $V_{th}$

$V_B = V_E + V_{BE}$, $V_E = V_B - V_{BE}$, Emitter Current: $I_E = \frac{V_E}{R_E}$

From o/p CKt or o/p loop $\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$ //..

Module - I
Chapter-2.

# BJT AC Analysis

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BJT transistor Modeling : In order to analyze the ac operation of a transistor amplifier it is necessary to develop an ac equivalent circuit of a transistor This ac equivalent circuit is called the model of a transistor.

The model of a transistor is a combination of circuit elements properly choosen the best approximates actual behaviour of the transistor under specific operating conditions.

There are three models commonly used in the small signal ac analysis of transistor network

1. re model
2. The hybrid equivalent model
3. The hybrid $\pi$ model.

At low frequencies the junction capacitances of the transistor acts as open circuit due to their high reactance due to their high reactance at low frequencies small signal models donot consider the effect of junction capacitance

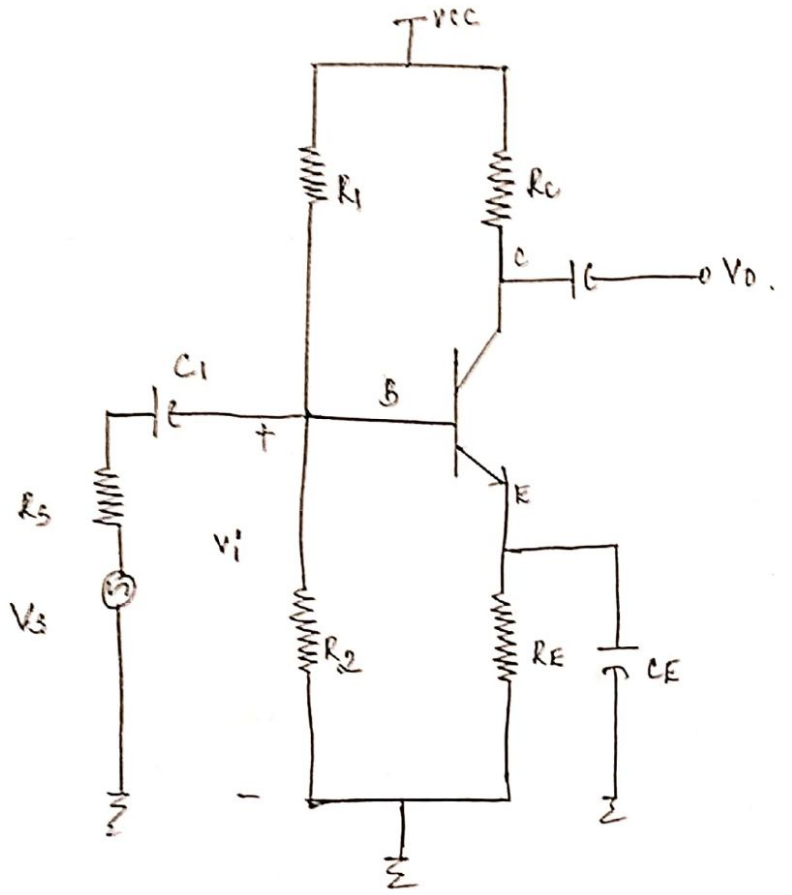
At high frequencies the junction capacitances conduct appreciably due to their low reactance providing feedback path from output to input in high frequencies small signal models considers the effect of junction capacitances.

re model : is a more practical model the important parameter re of this model is determined by the actual operating conditions rather than using data sheet values.

hybrid model : the transistor is modelled based on what is happening at its terminals without regard for the physical process taking place inside the transistor

Hybrid π model: hybrid π model will provide a more accurate model for high frequency effects. This model is used for a full frequency analysis.

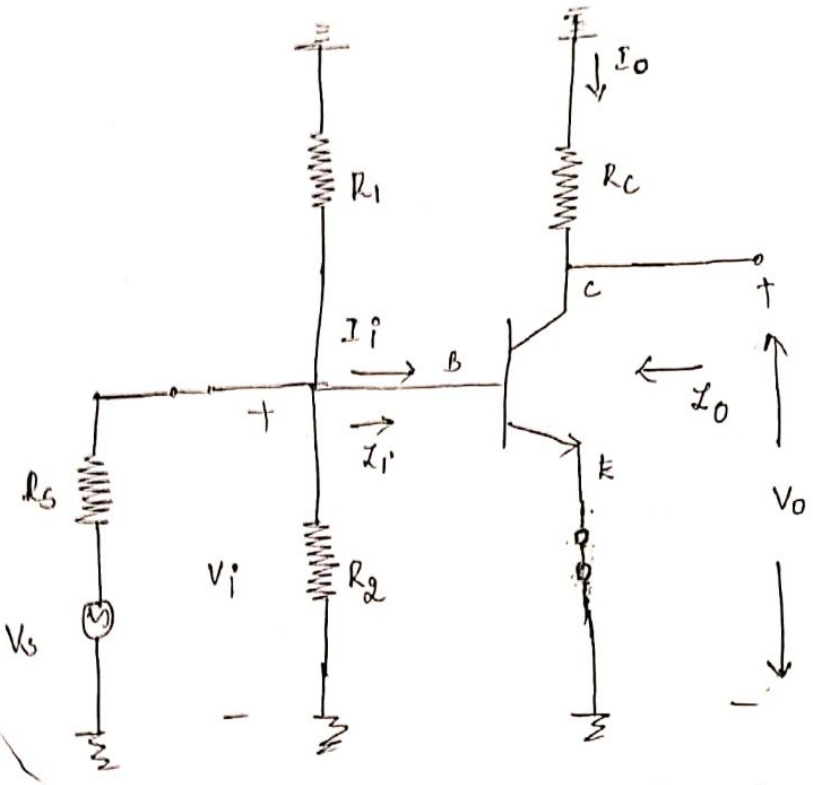
To demonstrate the effect that the ac equivalent circuit will have on the analysis to follow consider the circuit as shown below.



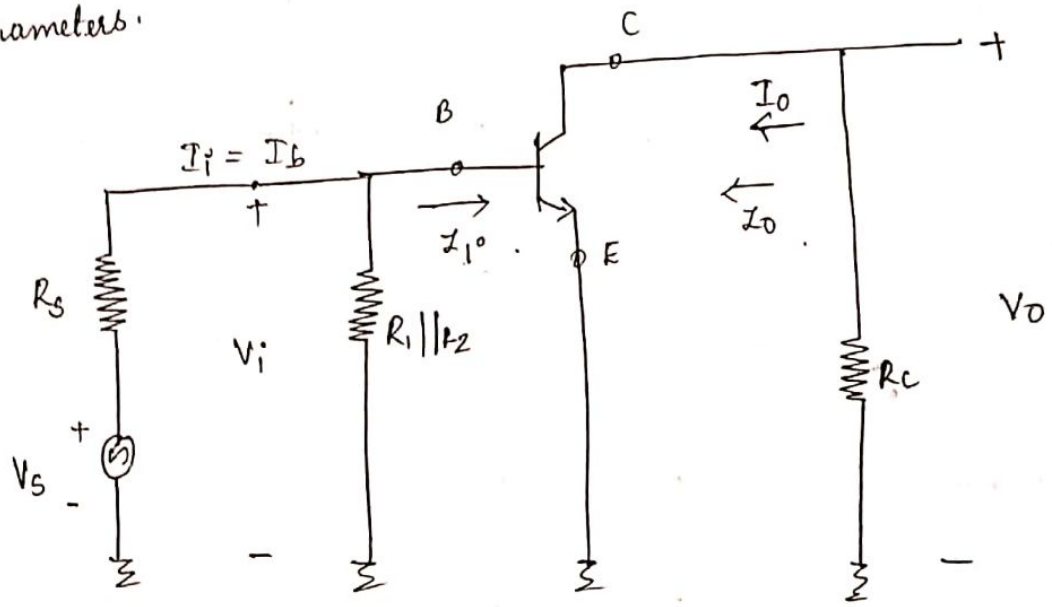

Since we are interested only in the ac response of the circuit all the dc supplies can be replaced by a zero potential equivalent i.e $V_{cc}=0$. The dc levels i.e Vcc were important for determining the proper Q-point of operation, once determined the dc levels can be ignored in the ac analysis of the network.

In addition the coupling capacitors $C_1$ and $C_2$ and bypass capacitor $C_E$ were short circuited due to the small reactance, resulting in short circuit the dc biasing resistor $R_E$.

The resulting equivalent circuit as shown below.




In ac Equivalent circuit analysis we have to determine $Z_i$, $Z_o$, $A_V$, $A_I$ parameters.




Small Signal ac analysis.

From the circuit $I_i = I_b$, $I_o = I_C$. Setting all dc sources to zero and replacing them by a short circuit equivalent.
Replacing all capacitors by a short circuit equivalent. Redrawing the network in a more convenient and logical form.

## The $r_e$-transistor model :

Common base configuration :- Common base BJT transistor has been replaced by the $r_e$ model. The transistor action in this configuration has been replaced by a single diode between emitter and base terminals and controlled current source between base and collector terminals.

for ac response the diode can be replaced by its equivalent ac resistance The ac resistance of a diode can be determined by the equation $r_{ac} = \frac{26mV}{I_D}$.

where $I_D$ is the dc current through the diode. Therefore representing $r_e = \frac{26mV}{I_E}$

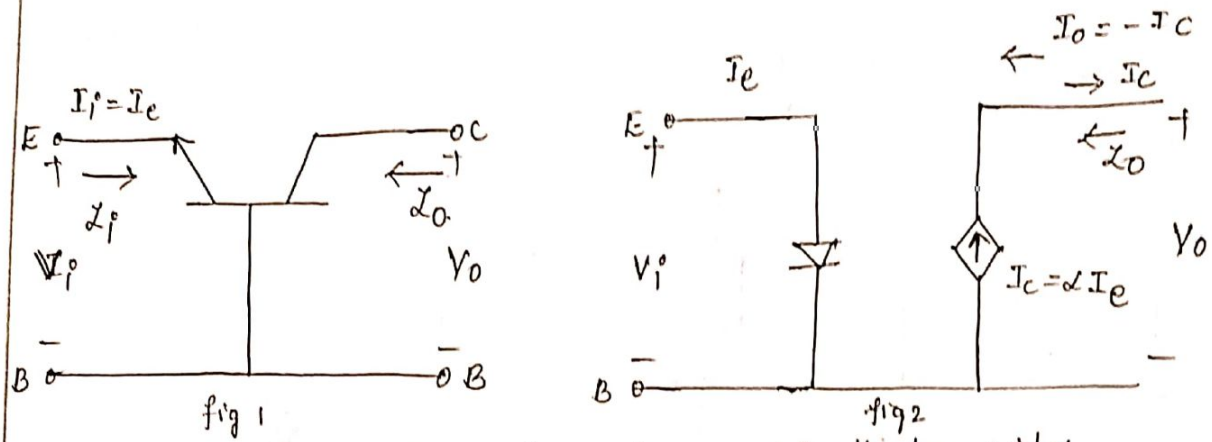



fig 1 fig 2

Common-Base BJT transistor and $r_e$-model of the transistor

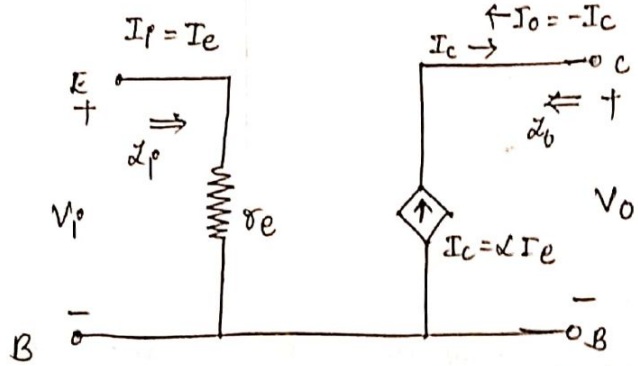



fig -3 Common-Base $r_e$ - equivalent model.

The subscript e of $r_e$ was chosen to emphasize that is the dc level of emitter current that determines the ac level of the resistance of the diode

Refer to the relation that exists for the input and output circuits of figure 3 it should be fairly obvious

Input impedance for the common base configuration of transistor is

$$Z_i = r_e$$

* for common base configuration typical values of $Z_i$ range from a few ohms to a maximum of about 50Ω *

Output Impedance : for o/p impedance if we set the signal $V_i = 0$, then $I_e = 0A$ and $I_c = \alpha I_e = \alpha \times 0A = 0$ resulting in an open circuit equivalence at the output terminals

$$Z_o = \infty \Omega$$

* for common-base configuration typical values of $Z_o$ are in Megaohm range *

In general for the common base configuration the input impedance is relatively small and output impedance is quite high.

Voltage gain: from the network of fig 3.

$$V_o = -I_o R_L$$

$$= -(-I_c) R_L$$

$$V_o = I_c R_L$$

$$V_o = \alpha I_e R_L$$

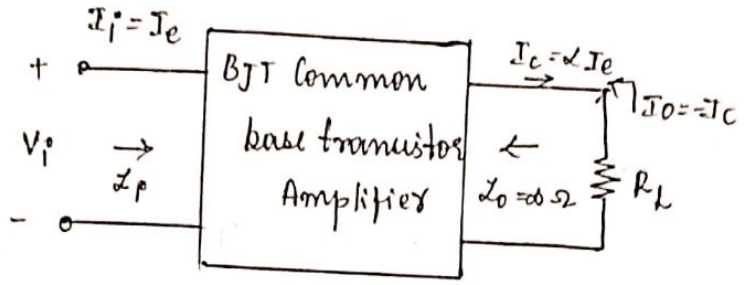
and $V_i = I_i Z_i = I_e Z_i = I_e r_e$

$$A_V = \frac{V_o}{V_i} = \frac{\alpha I_e R_L}{I_e r_e} = \frac{\alpha R_L}{r_e} \quad \text{if } \alpha = 1 \quad \boxed{A_V = \frac{R_L}{r_e}}$$

Current gain: $A_I = \frac{I_o}{I_i}$

$$A_I = \frac{I_o}{I_i} = \frac{-I_c}{I_e} = \frac{-\alpha I_e}{I_e} = -\alpha$$

$$\boxed{A_I = -\alpha}$$




Eg ① For a common-base configuration with $I_E = 4\,mA$, $\alpha = 0.98$ and an ac signal of 2mV applied b/w the base and emitter terminals.

(a) Determine the input impedance

(b) Calculate the voltage gain if a load of $0.56\,K\Omega$ is connected to the o/p terminals.

(c) Find the output impedance and current gain

$\rightarrow r_e = \frac{26\,mV}{I_E} = \frac{26\,mV}{4\,mA} = 6.5\,\Omega$ , $Z_i = r_e = 6.5\,\Omega$

$\rightarrow I_i = I_e = \frac{V_i}{Z_i} = \frac{2\,mV}{6.5\,\Omega} = 307.69\,\mu A$

$\rightarrow V_o = I_c R_L = \alpha I_e R_L = 0.98 \times 307.69\,\mu A \times 0.56\,K\Omega = 168.86\,mV$

$A_V = \frac{V_o}{V_i} = \frac{168.86\,mV}{2\,mV} = 84.43$ . $A_I = \frac{I_o}{I_i} = -\alpha = -0.98$

$\rightarrow Z_o = \infty\,\Omega$

**Common-emitter Configuration** : For Common-emitter configuration the input terminals are base and emitter terminals. and output terminals are collector and emitter terminals. Replacing the re Equivalent model. the Controlled current source is connected between the collector and base terminals and the diode between the base and emitter terminals.

In CE Configuration the base current is the input current whereas output current is $I_C$

$$I_C = \beta I_b$$

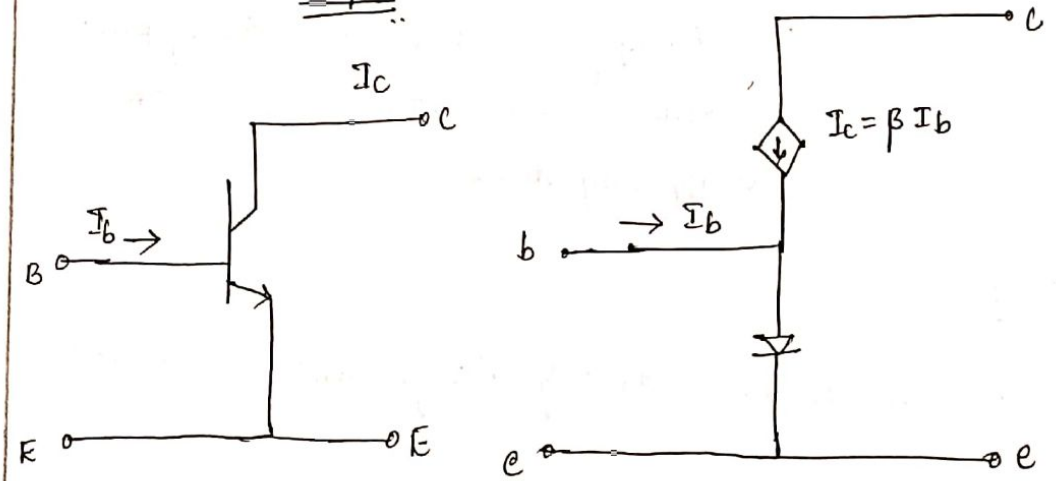
The current through the diode is therefore determined by

$$I_e = I_C + I_b$$

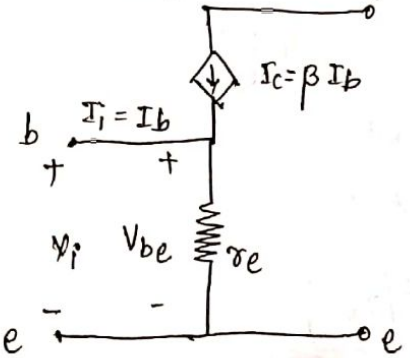
$$I_e = \beta I_b + I_b = I_b(1+\beta)$$

$$\boxed{I_e = I_b(1+\beta)}$$ if $\beta$ is very much greater than 1 then $1+\beta = \beta$

$$I_e = \beta I_b$$




Common-emitter BJT transistor and Approximate model CE Configuration




$r_e$ - Equivalent model

**Input Impedance of CE Configuration**

$$Z_i = \frac{V_i}{I_i} = \frac{V_{be}}{I_b}$$

using ohms law

$$V_i = V_{be} = I_e r_e = (I_c + I_b) r_e = (\beta I_b + I_b) r_e$$

$$V_{be} = V_i = (\beta + 1) I_b r_e$$

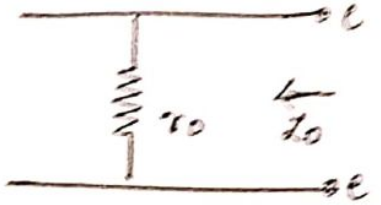
$$Z_i = \frac{V_{be}}{I_b} = \frac{(\beta+1) I_b r_e}{I_b}$$

$$Z_i = (\beta + 1) r_e, \quad \boxed{Z_i = \beta r_e}$$

$\beta + 1 \cong \beta$

for the common-emitter configuration, $Z_i$ defined by $\beta r_e$ same from two hundred ohms to the kilohm range with resistance of about $0.1\,k\Omega$ to $1\,k\Omega$.

Output impedance : from the graphical analysis of the data sheet values negligible resistance exist b/w collector and emitter.




For CE configuration circuit if the applied signal is set to zero the current $I_c = 0$ and op impedance is

$$\boxed{Z_o = r_o}$$

If $r_o$ is ignored as in the $r_e$-model the output impedance is defined by $Z_o = \infty\,\Omega$.

Gain: $A_v = \frac{V_o}{V_i}$

$V_o = -I_o R_L$

$= -I_c R_L$

$V_o = -\beta I_b R_L$.

$V_i = I_i Z_i = I_b \beta r_e$

$A_v = -\frac{\beta Z_b R_L}{\beta Z_b r_e}$

$$\boxed{A_v = -R_L / r_e}$$

Current gain $A_I = \frac{I_o}{I_i}$

$$A_I = \frac{I_C}{I_b} = \frac{\beta I_b}{I_b}$$

$$\boxed{A_I = \beta}$$

Eg 2: Given $\beta = 120$, $I_E = 3.2\,mA$ for CE Configuration with $r_o = \infty\,\Omega$ determine $Z_i$, $Z_o$, $A_V$, $A_I$ with $2K\Omega$ load resistor.

Solution: $r_e = \frac{26mV}{I_E}$

$$r_e = \frac{26mV}{3.2mA} = 8.125\,\Omega$$

$$Z_i = \beta r_e = 120 \times 8.125\,\Omega = 975\,\Omega$$

$$A_V = -\frac{R_L}{r_e} = \frac{2K\Omega}{8.125\,\Omega} = -246.15$$

$$A_I = \frac{I_o}{I_p} = \beta = 120$$

For Common Collector Configuration: Replace the Emitter terminal with Collector and Viceversa.

## Common-emitter fixed bias using re-model

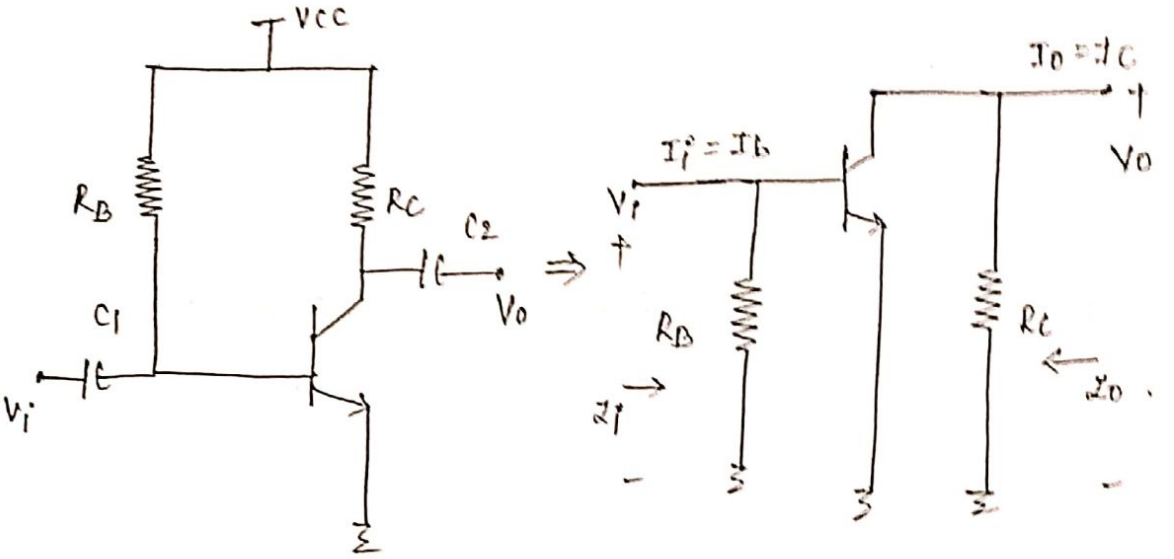
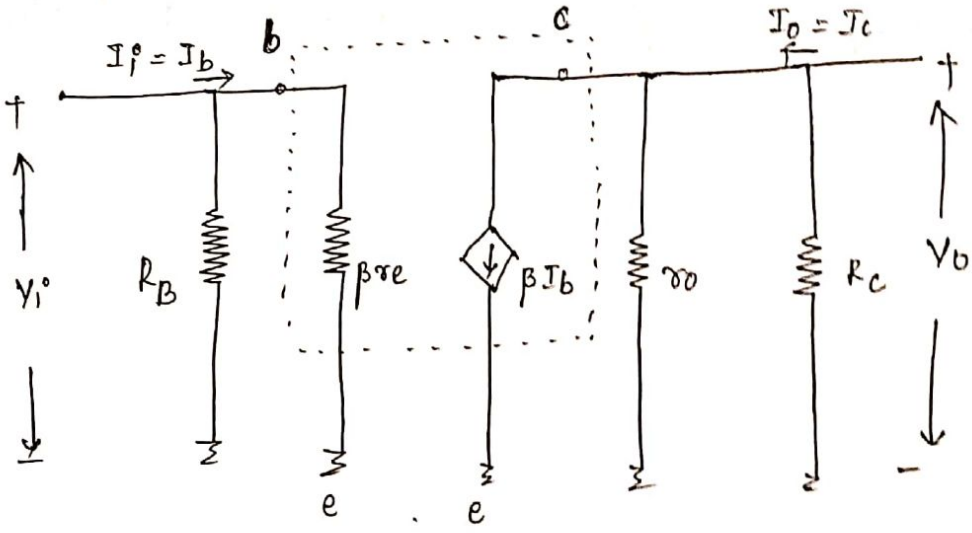



figure above shows the common-emitter amplifier using the fixed bias the input signal $v_i$ is applied to the base of transistor through input coupling capacitor $C_1$ the amplified signal $v_i$ is taken out the collector through the output coupling capacitor $C_2$.

In order to perform the small signal ac analysis let us obtain the ac equivalent circuit by reducing the dc source Vcc to zero and short circuiting the coupling capacitor.




Equivalent re-model.

Input Impedance :- From the circuit $Z_i$ is given by the parallel combination of $R_B$ and $\beta r_e$

$$Z_i = R_B \| \beta r_e$$

From the analysis of parallel elements that the total resistance of two parallel resistors is always less than the smallest and very to the smallest if one is much larger than other.

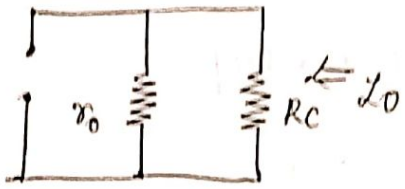
$R_B > \beta r_e$

$R_B \geq 10 \beta r_e$

$$Z_i = \beta r_e$$

$R_B \geq 10 \beta r_e$ .

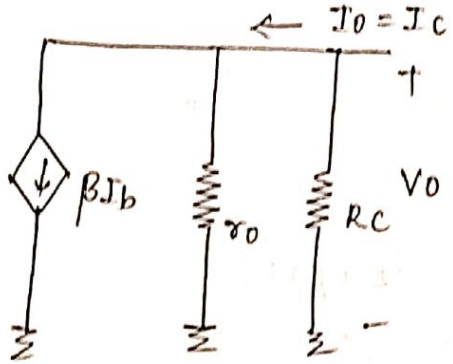
output Impedance : The o/p Impedance determined by Considering $V_i = 0$ when $V_i = 0$, $I_b = 0$, $I_i = 0$ resulting in open circuit.




$$Z_o = r_o \| R_C$$

$r_o \geq 10 R_C$

Voltage gain: $A_v = V_o / V_i$ Consider the output circuit.




o/p ckt

$$V_o = -I_o \cdot R_L$$

$$= -I_c \cdot (r_o \| R_C)$$

$$V_o = -\beta I_b (r_o \| R_C)$$

From the i/p circuit Apply KVL to b-e loop we get

$$V_i - I_b \beta r_e = 0$$

$$V_i = I_b \beta r_e$$

$$I_b = V_i / \beta r_e$$

$$V_o = -\beta \cdot I_b (r_o \| R_c)$$

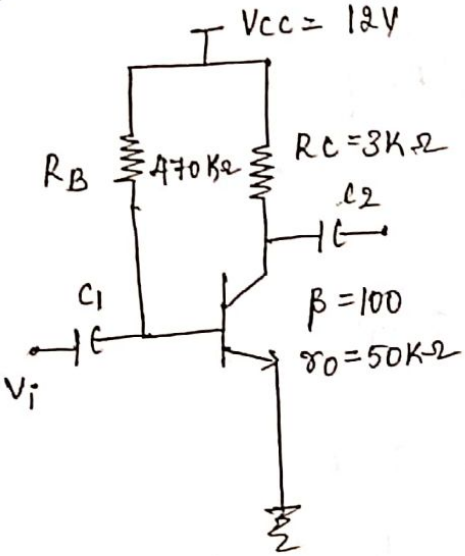
$$= -\beta \cdot \frac{V_i}{\beta r_e} (r_o \| R_c)$$

$$\frac{V_o}{V_i} = -\frac{r_o \| R_c}{r_e}$$

$$\boxed{A_V = -\frac{r_o \| R_c}{r_e}}$$

The negative sign in the resulting equation $A_V$ reveals that a 180° phase shift occurs b/w the input and output signals.

Eg: For the network shown below determine $r_e$, $Z_i$, $Z_o$, $A_V$




DC Analysis

Apply KVL to B-E loop

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{470K}$$

$$\boxed{I_B = 24.04 \mu A}$$

$$I_E = I_C + I_B$$

$$= \beta I_B + I_B = I_B (\beta + 1)$$

$$I_E = 24.04 \mu A (100 + 1)$$

$$\boxed{I_E = 2.428 mA}$$

$$r_e = \frac{26 mV}{I_E} = \frac{26 mV}{2.428 mA} = 10.71 \Omega$$

$\beta r_e = 100 \times 10.71\Omega = 1.071\Omega$

$Z_i = R_B \| \beta r_e = (470K \| 1.071\Omega) = 1.07K\Omega$

$Z_o = R_C = 3K\Omega$

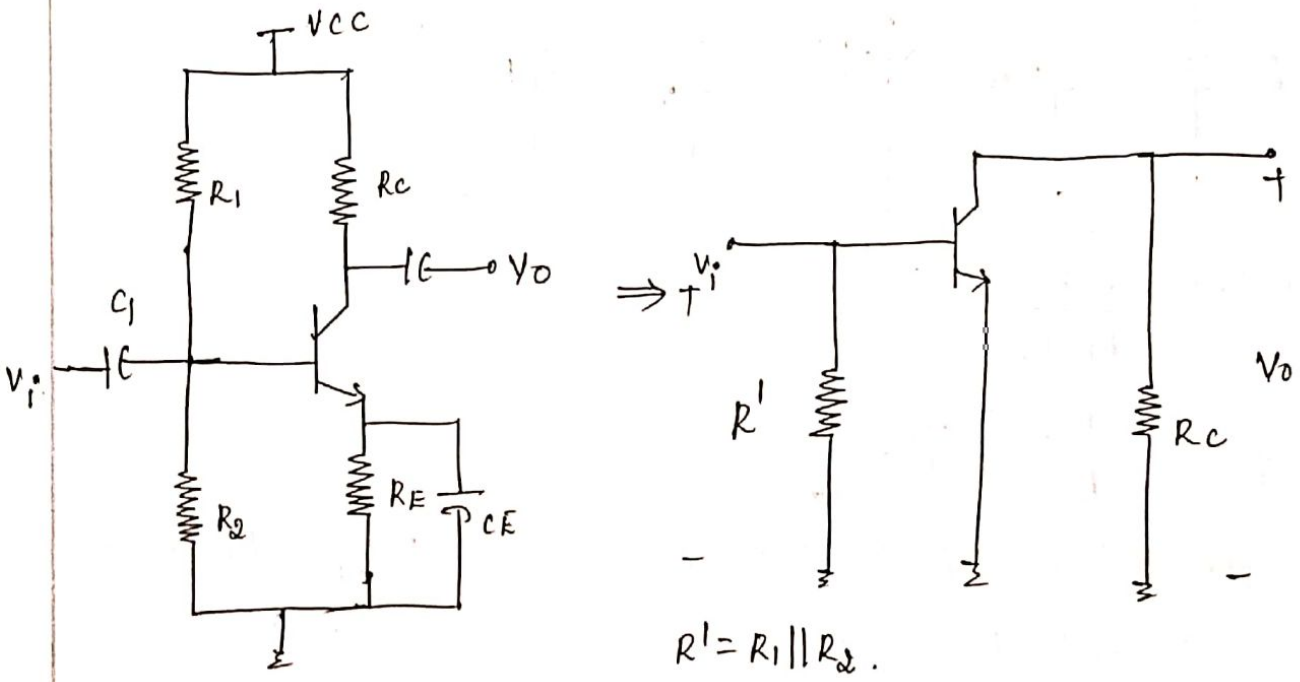
$$A_V = -\frac{R_C}{r_e} = \frac{3K\Omega}{10.71\Omega} = -280.11$$

and

output Impedance, $Z_o = r_o \| R_C = 50K\Omega \| 3K\Omega = 2.83K\Omega$

$$A_V = -\frac{R_C \| r_o}{r_e} = -264.24$$

Voltage divider bias : CE Configuration using voltage divider bias.



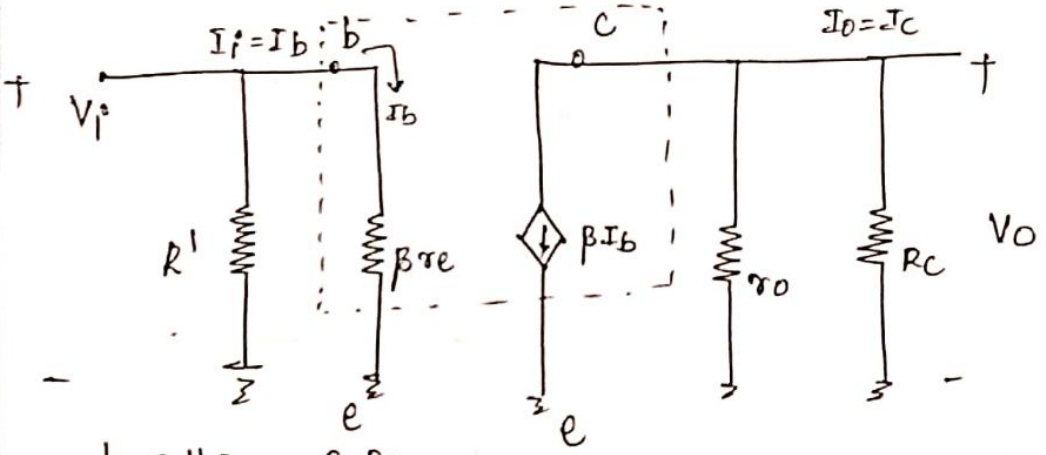

$R' = R_1 \| R_2$.

The ac input signal $V_i$ is applied to the base of the transistor through the input coupling capacitor $C_1$. The amplified signal $V_o$ is taken out the collector through the output coupling capacitor $C_2$. The emitter bypass capacitor $C_E$ is used to prevent the loss of voltage due to ac negative feedback through $R_E$ by creating an ac ground at the emitter.

At the low frequency the coupling capacitors $C_1$, $C_2$ and bypass capacitor $C_E$ is short circuited.

To perform the small signal ac analysis the equivalent ckt by reducing $V_{cc}$ to zero and replace capacitors by short circuit.

$R_1$ appears b/w base and ground thus $R_1$ comes in parallel with $R_2$ and $R_C$ appears b/w collector and ground. $R_E$ parallel with short circuit of $C_E$. Due to low impedance across emitter $R_E$ is also short circuited.




$$R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Input Impedance: $\boxed{Z_i = R' \| \beta r_e}$

Output Impedance: $Z_o$, $V_i = 0$, $I_i = 0$, $I_b = 0$ therefore till $\beta I_b$ the ckt is acting as open circuit

$$\boxed{Z_o = R_C \| r_o}$$

Gain: $A_V = \frac{V_o}{V_i}$

$$V_o = -I_o (R_C \| r_o)$$

$$= -I_c (R_C \| r_o)$$

$$V_o = -\beta I_b (R_c \| r_o)$$

$$= -\beta \cdot \frac{V_i}{\beta r_e} (R_c \| r_o)$$

$$\frac{V_o}{V_i} = \frac{-(R_c \| r_o)}{r_e}$$

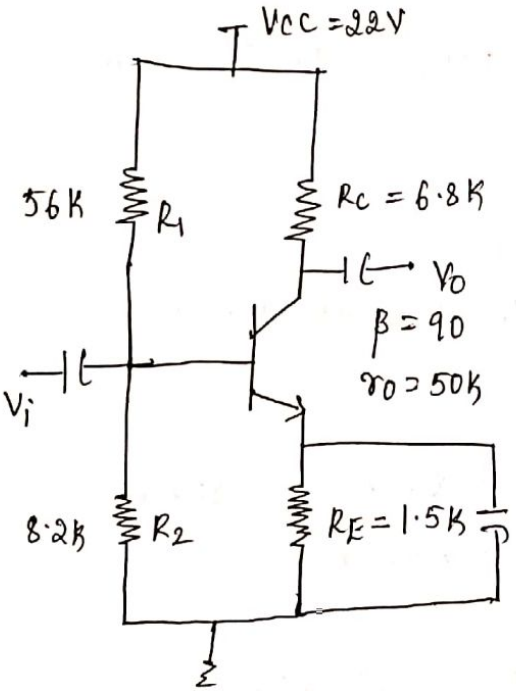
$$\boxed{A_V = \frac{-R_c \| r_o}{r_e}}$$

wkt from b-e loop

$$I_b = \frac{V_i}{\beta r_e}$$

Negative sign indicates the phase shift b/w input and output.

Eg:4 For the given n/w determine $Z_i$, $Z_o$, $A_V$. [ If $r_o$ is not given consider $r_o = \infty \Omega$ and neglect).




DC Analysis to find $I_E$

$$\beta R_E \geq 10 R_2$$

$$90 \times 1.5K \geq 10 \times 8.2K$$

$$135K \geq 82K \text{ (Satisfied)}$$

using Approximate analysis.

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{22V \times 8.2K}{56K + 8.2K} = 2.81V$$

$$V_E = V_B - V_{BE} = 2.81V - 0.7 = 2.11V$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11V}{1.5K\Omega} = 1.41mA$$

$$r_e = \frac{26mV}{I_E} = \frac{26mV}{1.41mA} = 18.44\Omega$$

$$R' = R_1 \| R_2 = R_1 R_2 / R_1 + R_2 = 56K \| 8.2K = 7.15K\Omega$$

$\beta r_e = 90 \times 13.44\,\Omega$

$\beta r_e = 1.66\,K\Omega$

$Z_i = R' \| \beta r_e$

$= 7.15K\Omega \| 1.66K\Omega$

$\boxed{Z_i = 1.35K\Omega}$

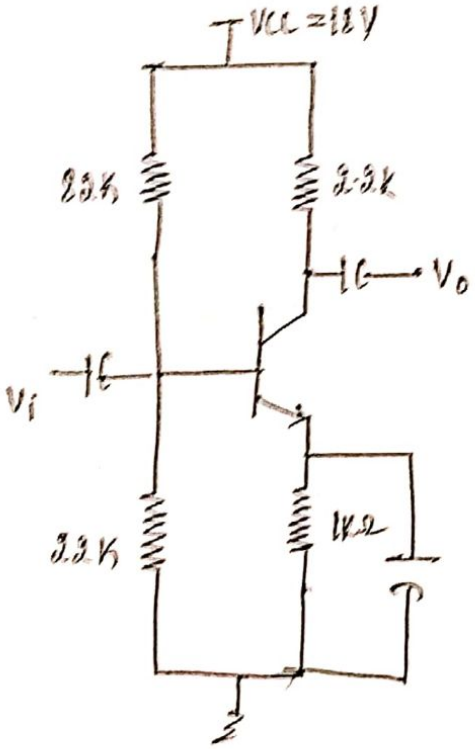
$Z_o = R_c \| r_o = 6.8K \| 50K$

$\boxed{Z_o = 5.98K\Omega}$

$A_v = \dfrac{-R_c \| r_o}{r_e} = \dfrac{-5.98K\Omega}{13.44\,\Omega}$

$\boxed{A_v = -334.3}$

⇒ A voltage divider biased amplifier has $\beta = 100$ and determine the $Z_i$, $Z_o$, $A_V$




$\beta R_E \geq 10 R_2$

$100 \times 1K\Omega \geq 10 \times 22K$

$100K \geq 220K$ condition not satisfied

use exact analysis.

$V_{th} = \dfrac{V_{CC} R_2}{R_1 + R_2} = \dfrac{18 \times 22K}{82K + 22K} = 3.807\,V$

$R_{th} = R_1 \| R_2 = \dfrac{R_1 R_2}{R_1 + R_2} = 17.346\,K\Omega$

$I_B = \dfrac{V_{th} - V_{BE}}{R_{th} + (1+\beta) R_E}$

$\boxed{I_B = 26.28\,\mu A}$

$I_E = I_B(1+\beta)$

$= 26.25\,\mu A(101)$

$\boxed{I_E = 2.65\,mA}$

$$r_e = \frac{26mV}{I_E}$$

$$r_e = \frac{26mV}{2.65mA} = 9.81\Omega$$

$\beta r_e = 100 \times 9.21$

$\beta r_e = 921$

$R' = R_{th} = R_1 || R_2$

$$Z_i = R' || \beta r_e$$

$= 17.346K || 921$

$\boxed{Z_i = 920.43\Omega}$

$Z_o = R_c || r_o$ , Neglect $r_o$

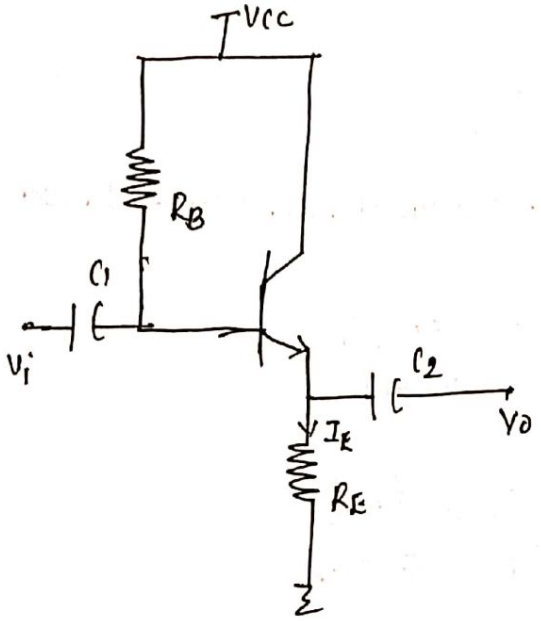
$\boxed{Z_o = 2.2K\Omega}$

$$A_V = \frac{-R_c || r_o}{r_e}$$

$$A_V = \frac{-2.2K}{9.81}$$

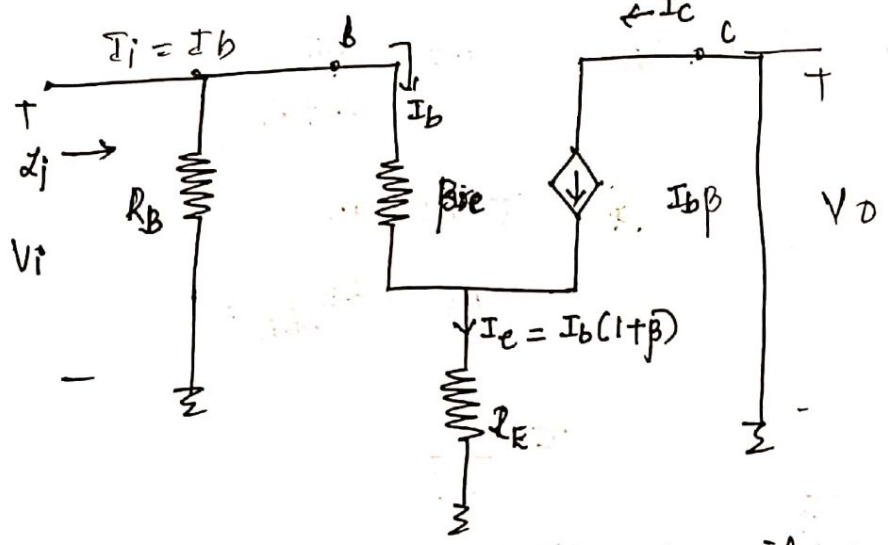
$\boxed{A_V = -224.2}$

**Emitter follower Configuration:** when the output is taken from the Emitter terminal of the transistor the network is referred as an Emitter follower




The output voltage is always slightly less than the input signal due to the drop from base to Emitter. The Emitter voltage is in phase with the signal $V_i$

It is frequently used for Impedance Matching it presents a high impedance at the input and a low impedance at the output which is opposite of the standard fixed bias Configuration.




Substituting the re equivalent circuit into the ac equivalent n/w

**Input Impedance:** Apply KVL to the i/p circuit we have

$$V_i = I_b \beta r_e + I_e R_E$$

$$= I_b \beta r_e + (1+\beta) I_b R_E$$

$$Z_b = \frac{V_i}{I_b} = \frac{I_b(\beta r_e + (1+\beta) R_E)}{I_b}$$

$$\boxed{Z_i = R_B \| Z_b}$$

$$\boxed{Z_b = \beta r_e + (1+\beta) R_E} = \beta r_e + \beta R_E = \beta (r_e + R_E) = \beta R_E$$

Output Impedance: Consider $I_b = \frac{V_i}{I_b}$

$$I_b = \frac{V_i}{Z_b} \qquad I_b = \frac{I_e}{1+\beta} \Rightarrow I_e = (1+\beta) I_b$$

$$\frac{I_e}{1+\beta} = \frac{V_i}{Z_b}$$

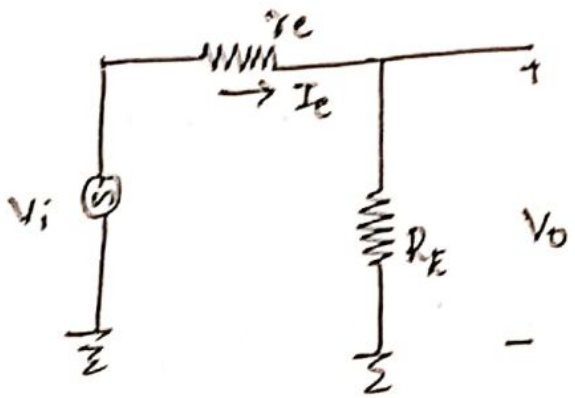
$$\frac{I_e}{1+\beta} = \frac{V_i}{Z_b}$$

$$I_e = \frac{V_i (1+\beta)}{Z_b}$$

$$I_e = \frac{V_i (1+\beta)}{\beta r_e + (1+\beta) R_E} = \frac{V_i \beta}{\beta (r_e + R_E)}$$

$$\boxed{I_e = \frac{V_i}{r_e + R_E}}$$

$$\boxed{V_i = I_e (r_e + R_E)}$$




To find $Z_o$: $V_i = 0$

$$Z_o = r_e \| R_E$$

$$Z_o = \frac{r_e R_E}{r_e + R_E}$$

$$A_V = \frac{V_o}{V_i}$$

Apply voltage divider rule to the output

$$V_o = \frac{R_E}{r_e + R_E} V_i$$

$$\frac{V_o}{V_i} = \frac{R_E}{r_e + R_E}$$

$$\boxed{A_V = \frac{R_E}{r_e + R_E}}$$

if $R_E >> r_e$

$$A_V = R_E / R_E = 1$$

$$A_I = \frac{I_o}{I_i}$$

$$I_i = \frac{V_i}{Z_i} \qquad I_o = \frac{-V_o}{R_E}$$

$$= \frac{V_o / R_E}{V_i / Z_i}$$

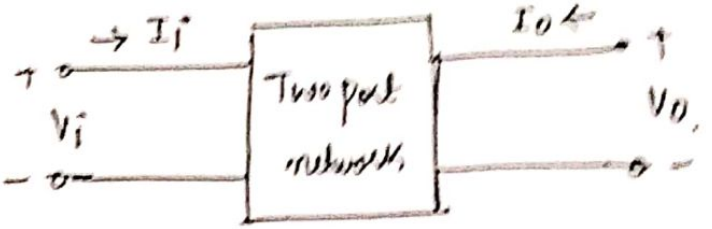
$$= \frac{V_o}{V_i} \times \frac{Z_i}{R_E}$$

$$\boxed{A_I = A_V \frac{Z_i}{R_E}}$$

## The hybrid equivalent model

Consider the two port network. To develop the hybrid equivalent model of two port network.

consider $I_i$ and $V_o$ are independent variables and $V_i$ and $I_o$ are dependent variables




$$V_i = h_{11} I_i + h_{12} V_o$$

$$I_o = h_{21} I_i + h_{22} V_o$$

The parameters $h_{11}, h_{12}, h_{21}$ and $h_{22}$ are called hybrid parameters or h-parameters. It is hybrid because the parameters are mix of impedance, admittance and dimensionless units

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0} \Rightarrow \text{Input impedance} = h_i$$

$$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0} \Rightarrow \text{Reverse voltage transfer ratio} = h_r$$

$$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0} \rightarrow \text{Forward voltage transfer ratio} = h_f$$

$$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0} \Rightarrow \text{output impedance} = h_o$$

$$V_i = h_i I_i + h_r V_o$$

$$I_o = h_f I_i + h_o V_o$$

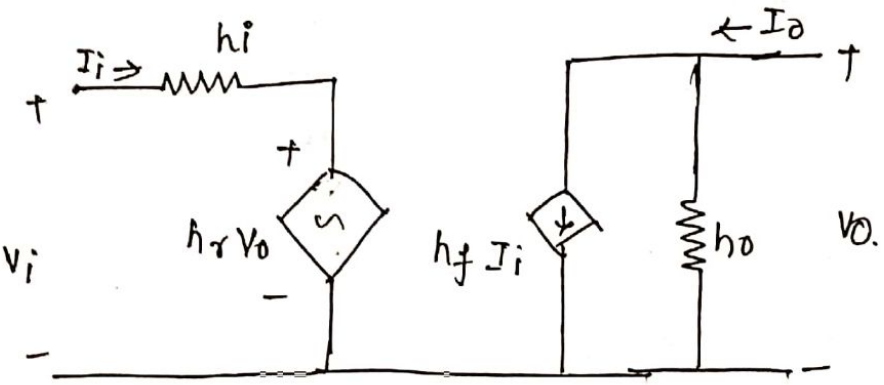
From the equation

$h_i I_i$ - represents the voltage drop across the impedance $h_i$

$h_r V_o$ - represents a controlled voltage source.

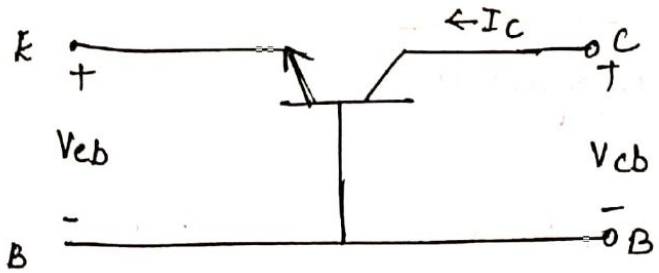
$h_f I_i$ - represents a controlled current source

$h_o V_o$ - represents the current through the admittance $h_o$.




hybrid equivalent model.

## Hybrid model of CB configuration




$h_i = h_{ib}$

$h_r = h_{rb}$

$h_f = h_{fb}$

$h_o = h_{ob}$

$V_i = V_{eb}$, $I_i = I_e$, $I_o = I_c$, $V_o = V_{cb}$

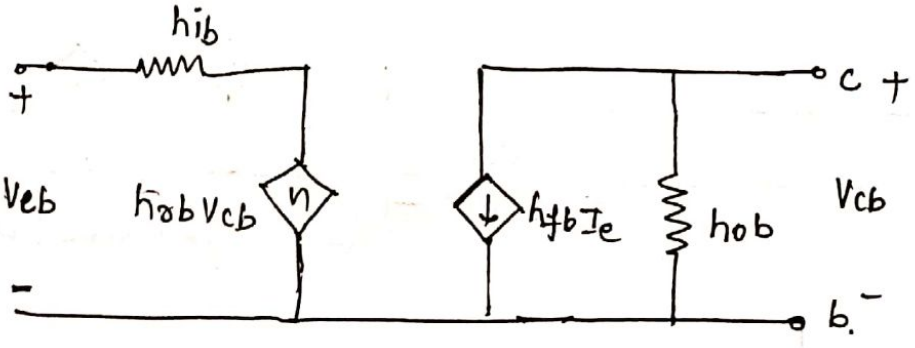
$V_i = h_i I_i + h_r V_o$

$I_o = h_f I_i + h_o V_o$

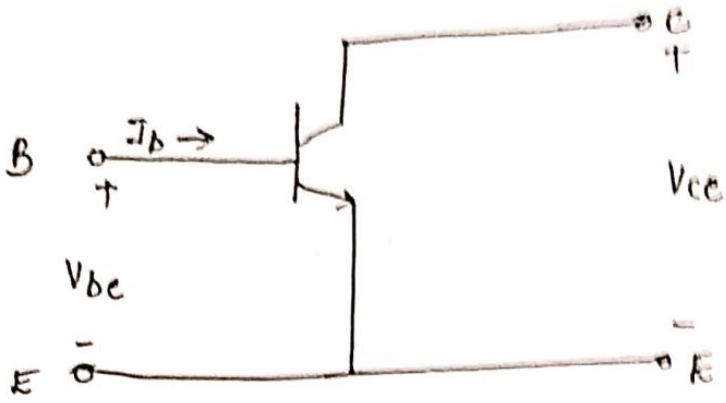
$\Rightarrow$

$V_{eb} = h_{ib} I_e + h_{rb} V_{cb}$

$I_c = h_{fb} I_e + h_{ob} V_{cb}$.



## Hybrid model for CE Configuration

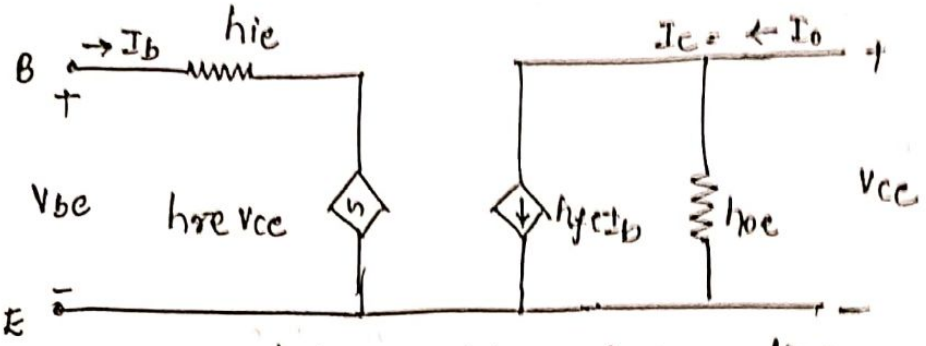



$h_i = h_{ie}$
$h_r = h_{re}$
$h_f = h_{fe}$
$h_o = h_{oe}$

$V_i = V_{be}$, $I_i = I_b$, $V_o = V_{ce}$, $I_o = I_c$.

$V_i = h_i I_i + h_r V_o \Rightarrow V_{be} = h_{ie} I_b + h_{re} V_{ce}$

$I_o = h_f I_i + h_o V_o \quad I_c = h_{fe} I_b + h_{oe} V_{ce}$



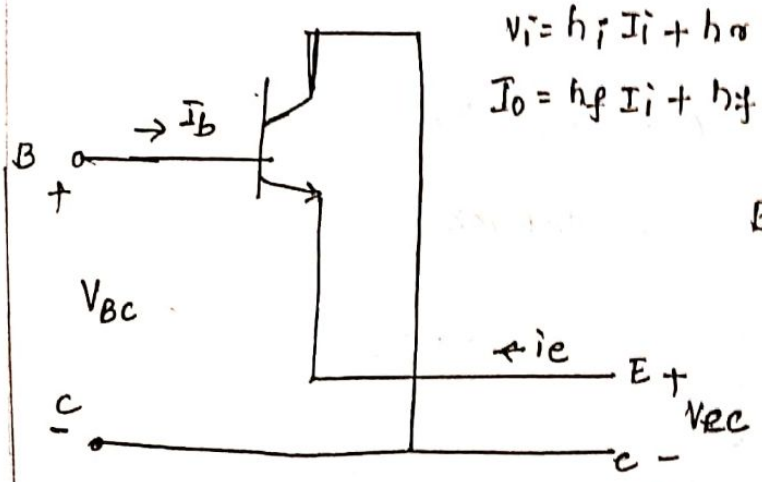

hybrid model of CE Configuration.

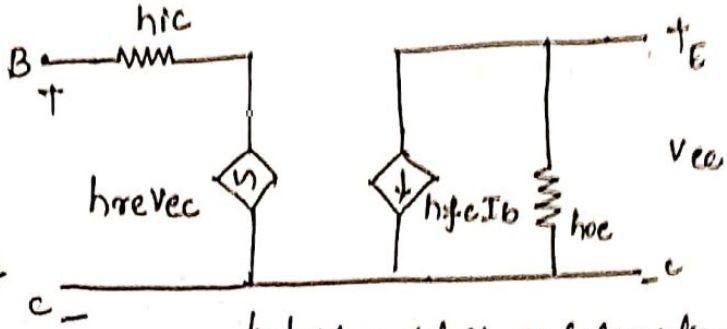
## Hybrid model for CC Configuration

$V_i = V_{bc}$, $V_o = V_{ec}$, $I_i = I_b$, $I_o = I_e$

$V_i = h_i I_i + h_r V_o \Rightarrow V_{bc} = h_{ic} I_b + h_{rc} V_{ec}$

$I_o = h_f I_i + h_f V_o \Rightarrow I_e = h_{fc} I_b + h_{oc} V_{ec}$




hybrid model of CC Configuration

# Common-Emitter fixed bias Configuration using h-parameters

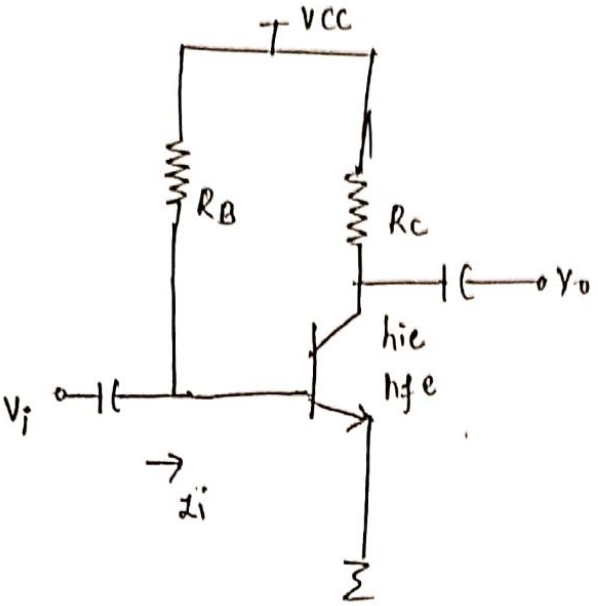
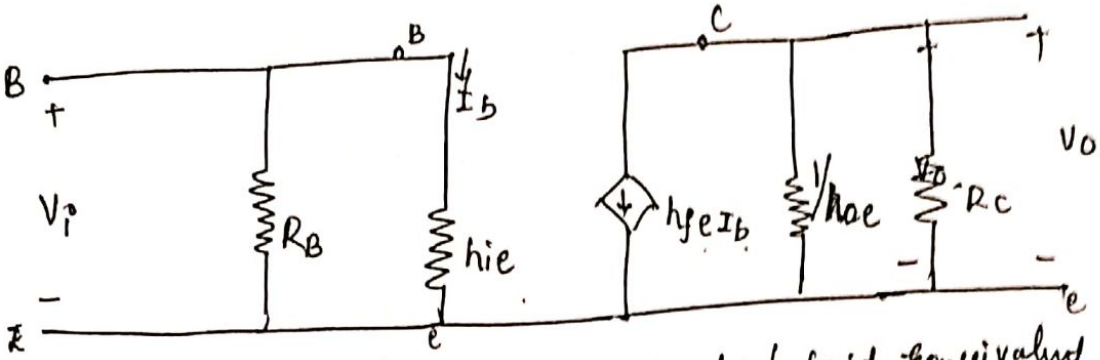



Figure shows the CE amplifier using fixed bias. The ac input signal $V_i$ is applied to the base of transistor through its input coupling capacitor $C_1$, the amplified signal $V_o$ is taken at the collector through the output coupling capacitor $C_2$.

For small signal ac analysis the dc source $V_{CC}$ will be equal to zero short circuit the coupling capacitor $C_1$ & $C_2$.

$R_B$ appears b/w base and ground $R_C$ b/w collector and ground.




Substituting the approximate hybrid equivalent circuit in ac equivalent N/W.

$$I_i = R_B \| h_{ie}$$

$$I_o = R_c \| 1/h_{oe}$$

Gain: $A_V = R_L = R_c \| 1/h_{oe}$ from ckt

$$V_o = -I_o R_L$$
$$= -I_c R_L$$
$$= -h_{fe} I_b R_L$$
$$= -h_{fe} \cdot \frac{v_i}{h_{ie}} R_L \qquad I_b = \frac{V_i}{h_{ie}}$$

$$A_V = \frac{V_o}{V_i} = \frac{-h_{fe}}{h_{ie}} R_L$$

$$\boxed{A_V = \frac{-h_{fe}}{h_{ie}} R_L} = \frac{-h_{fe}(R_c \| 1/h_{oe})}{h_{ie}}$$

## Common-Emitter fixed bias Configuration using h-parameters.

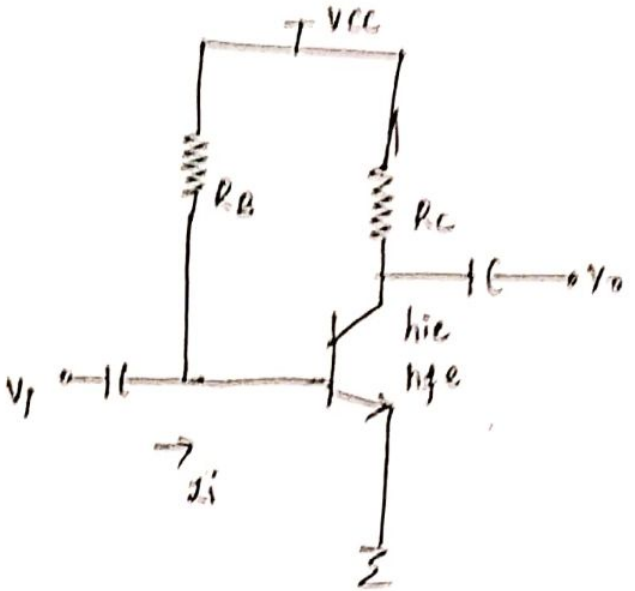
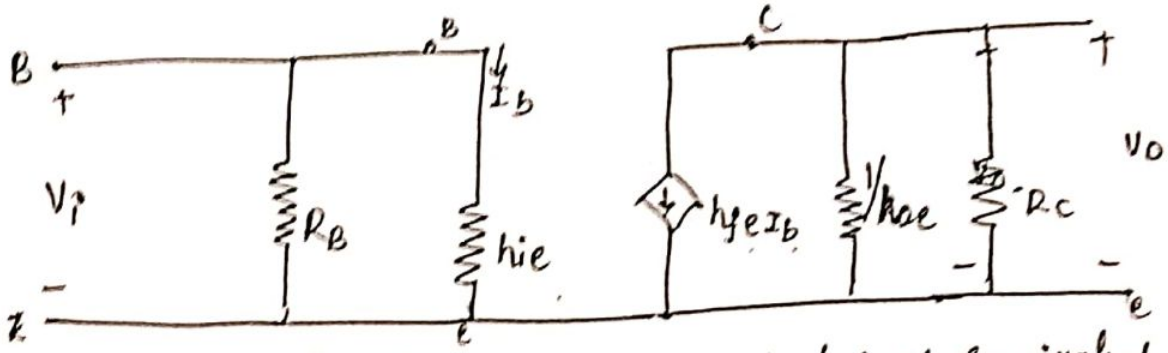



Figure shows the CE amplifier using fixed bias. The ac input signal $V_i$ is applied to the base of transistor through the input coupling capacitor $C_1$. The amplified signal $V_o$ is taken at the collector through the output coupling capacitor $C_2$.

For small signal ac analysis the dc source Vcc will be replaced by zero. Short circuit the coupling capacitor $C_1$ & $C_2$.

$R_B$ appears b/w base and ground $R_C$ b/w collector and ground.




Substituting the approximate hybrid equivalent circuit in ac equivalent N/W.

$$Z_i = R_B \| h_{ie}$$

$$Z_o = R_C \| 1/h_{oe}$$

Gain: $A_V = R_L' = R_C \| 1/h_{oe}$ from ckt

$$V_o = -I_o R_L$$
$$= -I_C R_L$$
$$= -h_{fe} I_b R_L$$
$$= -h_{fe} \cdot \frac{v_i}{h_{ie}} R_L \qquad I_b = \frac{V_i}{h_{ie}}$$

$$A_V = \frac{V_o}{V_i} = \frac{-h_{fe}}{h_{ie}} \frac{V_i}{V_i} R_L$$

$$\boxed{A_V = \frac{-h_{fe}}{h_{ie}} R_L} = \frac{-h_{fe}}{h_{ie}} (R_C \| 1/h_{oe})$$

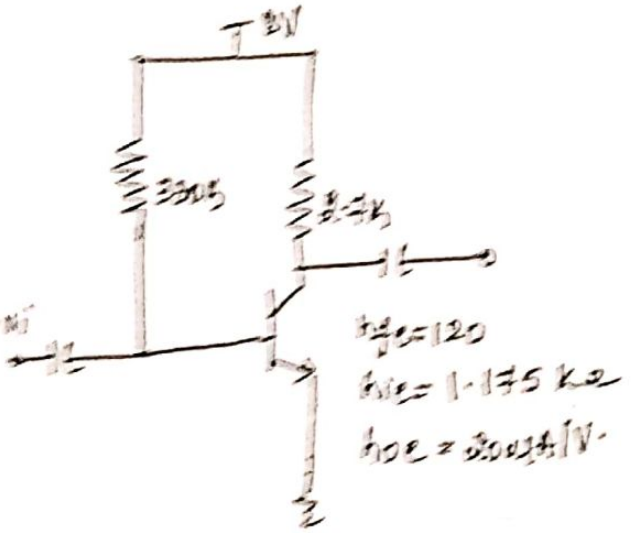
$$A_V = \frac{V_o}{V_i} = \frac{-h_{fe}(R_c \parallel 1/h_{oe})}{h_{ie}}$$

$A_i$ - Assuming that $R_B >> h_{ie}$

$$A_i = \frac{I_o}{I_i} = \frac{h_{fe} I_b}{I_i} = \frac{h_{fe} I_b}{I_b}$$

$$A_i = h_{fe}$$

To find the other parameters $Z_i, Z_o, A_V, A_i$




$Z_i = R_B \parallel h_{ie} = 330k \parallel 1.175\,k\Omega = 1.17k\Omega$

$r_o = 1/h_{oe} = \frac{1}{20\mu A/V} = 50k\Omega$

$Z_o = R_c \parallel \frac{1}{h_{oe}} = 2.7k \parallel 50k\Omega = 2.56k\Omega$

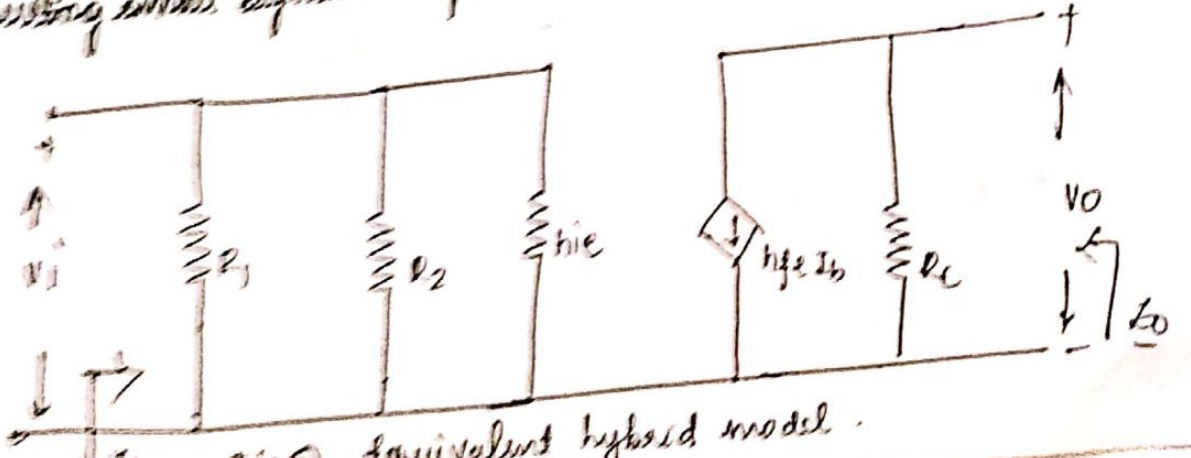
$$A_V = \frac{-h_{fe}(R_c \parallel 1/h_{oe})}{h_{ie}}$$

$$= -262.34$$

$A_i = h_{fe} = 120$ //.

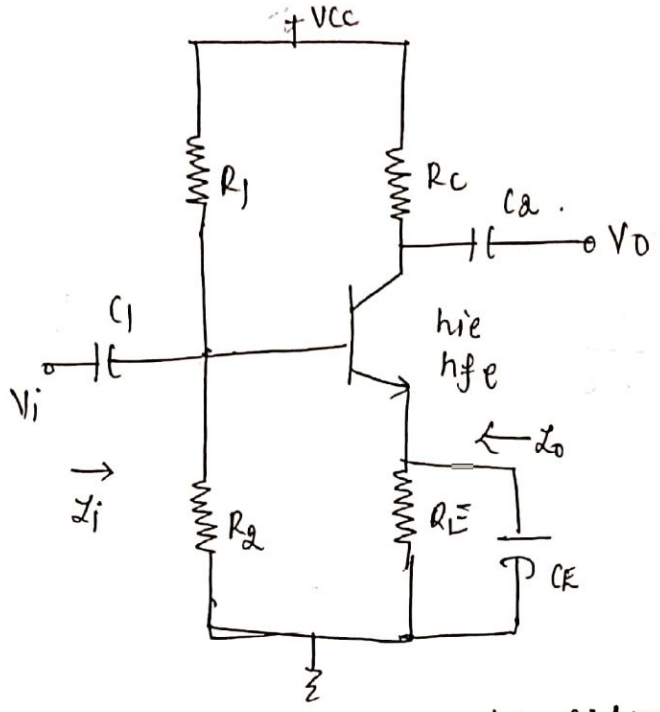
Voltage divider configuration : For this voltage divider bias configuration the

Assuming small signal ac equivalent $R_B$ is replaced with $R' = R_1 \parallel R_2$




Equivalent hybrid model.

(without bypass $R_E$)




Fig① Voltage divider bias configuration

The small signal parameter hre Vce is often too small to be considered so that input resistance is just hie often the output resistance hoe is often large compared with the collector resistor $R_c$ and its effects can be ignored.

Input impedance: ($Z_i$): The input impedance is the parallel combination of bias resistors $R_1$ & $R_2$ $\quad R' = R_1 \| R_2$

$$R' = \frac{R_1 R_2}{R_1 + R_2}$$

R' parallel with hie

$$\boxed{Z_i = R' \| hie}$$

Output impedance: As $h_{fe} I_b$ ($\beta I_b$) is an ideal current generator with infinite output impedance

$$\boxed{Z_o = R_c}$$

Voltage gain ($A_V$): The negative sign indicates phase inversion of the output waveform

$V_o = -I_o R_c$

$V_o = -h_{fe} I_b \cdot R_c$ $\qquad I_o = I_c = h_{fe} I_b$

$= -h_{fe} \frac{V_i}{h_{ie}} R_c$ $\qquad I_b = \frac{V_i}{h_{ie}}$

$$\boxed{V_o = -\frac{h_{fe}}{h_{ie}} V_i R_c}$$

$$A_V = \frac{V_o}{V_i}$$

$$= \frac{-\frac{h_{fe}}{h_{ie}} \cdot V_i R_c}{V_i}$$

$$\boxed{A_V = -\frac{h_{fe}}{h_{ie}} R_c}$$

Current gain: $A_I = \frac{I_o}{I_i}$

using current divider rule $\boxed{\frac{I_i R'}{R' + h_{ie}} = I_b}$

$I_o = -h_{fe} I_b$

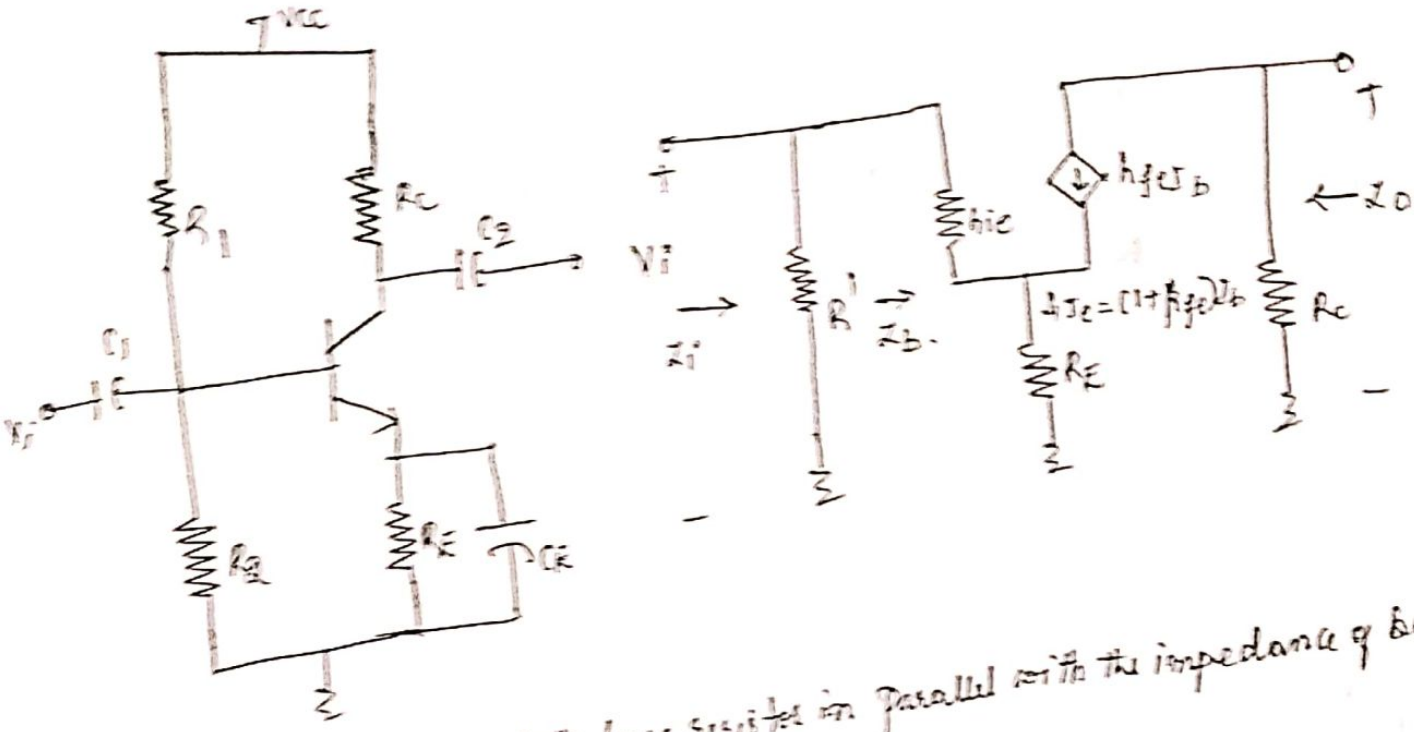
$$\boxed{\frac{I_o}{I_b} = -h_{fe}}$$

$$\boxed{\frac{I_b}{I_i} = \frac{R'}{R' + h_{ie}}}$$

$$\boxed{A_I = \frac{I_o}{I_i} \times \frac{I_b}{I_b} = -h_{fe} \cdot \frac{R'}{R' + h_{ie}}}$$

$$\boxed{A_I = h_{fe}}$$

With Bypass $R_E$




The input impedance $Z_i$ is the base resistor in parallel with the impedance of base

Apply KVL to the base transistor

$$V_i = I_b h_{ie} + I_E R_E$$

$$V_i = I_b h_{ie} + (1+\beta) I_b R_E \qquad \beta = h_{fe} I_b$$

$$V_i = I_b (h_{ie} + (1+\beta) R_E)$$

$$\boxed{V_i = I_b (h_{ie} + (1+h_{fe}) R_E}$$

$$Z_b = \frac{I_b (h_{ie} + (1+h_{fe}) R_E)}{I_b}$$

$$\boxed{Z_b = h_{ie} + (1+h_{fe}) R_E}$$

$$1 + h_{fe} = h_{fe}$$

$$\boxed{Z_b = h_{ie} + h_{fe} R_E}$$

$$R' = R_1 \| R_2$$

$$\boxed{Z_i = R' \| Z_b}$$

output impedance ($Z_o$) : Set $V_i = 0$, $I_b = 0$ therefore $\boxed{Z_o = R_C}$

Gain $A_V$ : $I_b = \frac{V_i}{Z_b}$

$V_0 = -I_0 R_C$

$= -I_C R_C$

$V_0 = -h_{fe} I_b R_C$

$V_0 = -h_{fe} \frac{V_i}{I_b} R_C$

$I_b = h_{ie} + h_{fe} R_E$

$\boxed{I_b = h_{fe} R_E}$

$A_V = \frac{V_0}{V_i}$

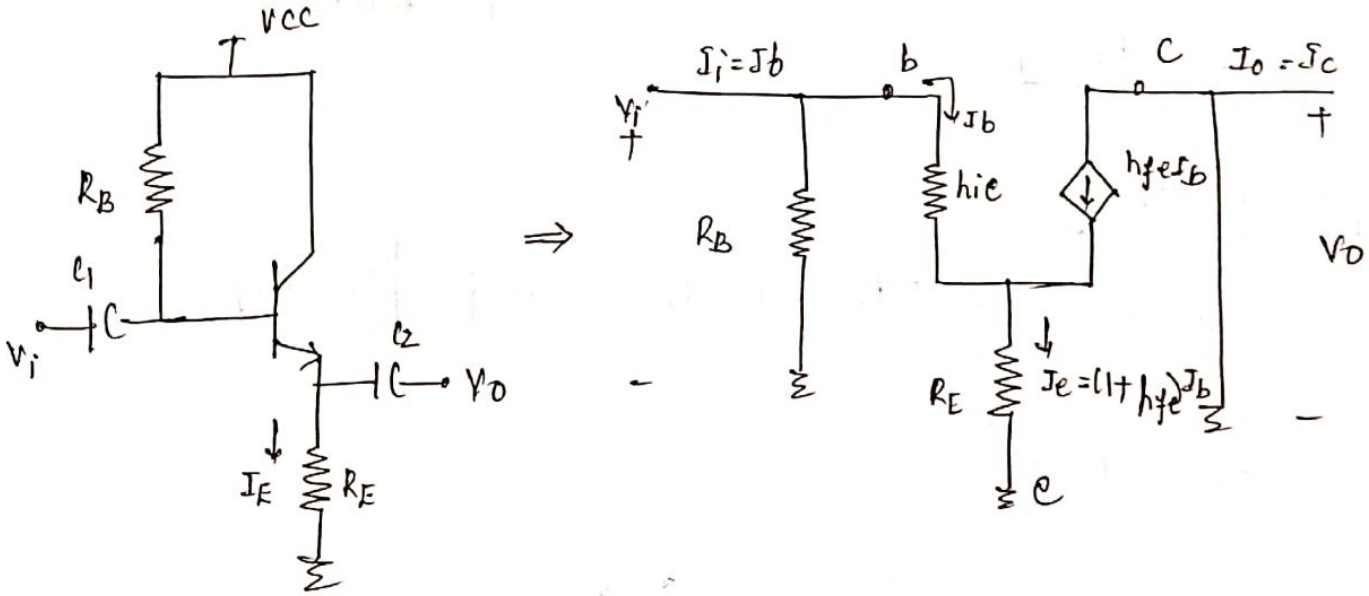
$= -h_{fe} \cdot \frac{V_i}{I_b} R_C \Big/ V_i$

$\boxed{A_V = -\frac{h_{fe} R_C}{I_b}}$

$A_V = -\frac{h_{fe} \cdot R_C}{h_{fe} R_E}$

$\boxed{A_V = -R_C / R_E}$

## Emitter follower Circuit



Input Impedance: $Z_i$

$$Z_i = R_B \| Z_b$$

$$Z_b = \frac{V_i}{I_b}$$

Apply KVL to b-e loop

$$V_i - I_b h_{ie} - I_e R_E = 0$$

$$V_i - I_b h_{ie} - I_b (1+h_{fe}) R_E = 0$$

$$V_i - I_b (h_{ie} - (1+h_{fe}) R_E) = 0$$

$$V_i = I_b (h_{ie} + (1+h_{fe}) R_E)$$

$$Z_b = \frac{V_i}{I_b} = \frac{I_b (h_{ie} + (1+h_{fe}) R_E)}{I_b}$$

$$\boxed{Z_b = h_{ie} + (1+h_{fe}) R_E}$$

$h_{ie}$ is very much small compared with $(1+h_{fe}) R_E$ so Neglect $h_{ie}$

$$Z_b = (1+h_{fe}) R_E$$

$$\boxed{Z_b = h_{fe} R_E}$$

$1+h_{fe} \simeq h_{fe}$.

Output Impedance: Consider $Z_b = \frac{V_i}{I_b}$ & $I_e = I_b (1+h_{fe})$

$$I_b = \frac{V_i}{Z_b} \rightarrow (1) \qquad I_b = \frac{I_e}{1+h_{fe}} \rightarrow (2)$$

Compare equation ① & ②

$$\frac{V_i}{Z_b} = \frac{I_e}{1+h_{fe}}$$

$$I_e = \frac{V_i(1+h_{fe})}{Z_b}$$

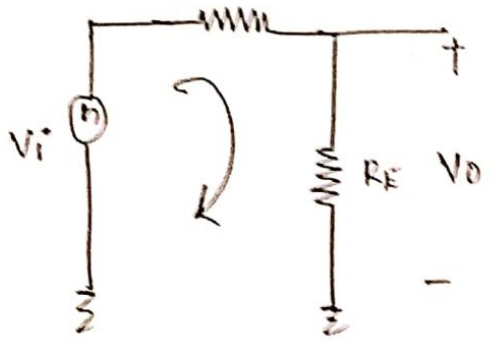
$$I_E = \frac{V_i(1+h_{fe})}{h_{ie} + (1+h_{fe})R_E}$$

$$I_e = \frac{V_i(1+h_{fe})}{\left(\frac{h_{ie}}{1+h_{fe}} + R_E\right)(1+h_{fe})}$$

$$I_e = \frac{V_i}{\frac{h_{ie}}{1+h_{fe}} + R_E}$$

$$\boxed{V_i = I_e\left(h_{ie}/1+h_{fe} + R_E\right)}$$

$h_{ie}/1+h_{fe}$




Set $V_i = 0$, $I_i = 0$, ∴ we get

$$Z_o = \frac{h_{ie}}{1+h_{fe}} \| R_E$$

if $1+h_{fe} \approx h_{fe}$

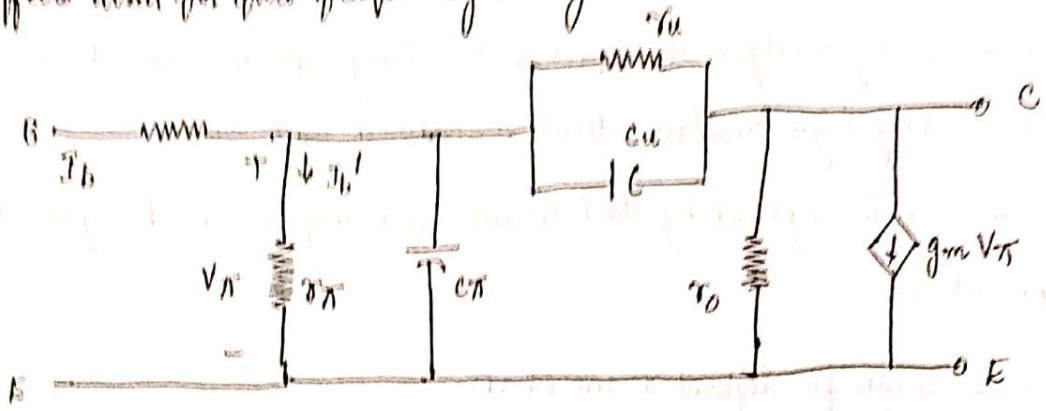
$$\boxed{Z_o = \frac{h_{ie}}{h_{fe}} \| R_E}$$

Apply voltage divider rule to the o/p

$$V_o = \frac{V_i R_E}{R_E + \frac{h_{ie}}{1+h_{fe}}}$$

$$A_V = \frac{V_o}{V_i} = \frac{R_E}{R_E + h_{ie}/1+h_{fe}}$$

Hybrid π model: Hybrid π model is more accurate model for high frequency effects used for full frequency analysis




Giacoll ect or hybrid π model high frequency transistor
Small signal ac equivalent circuit.

$$g_m V_\pi = g_m (I_b' r_\pi) = g_m I_b' \beta r_e$$

$$= \frac{1}{r_e} I_b' \beta r_e$$

$$g_m V_\pi = \underline{\beta I_b'}.$$

All the capacitors that appears in the above figure are stray parasitic capacitors between the various junction of the device.

At high frequency all capacitive effects will come into play, at low frequency all capacitance acts as open circuit.

$C_\pi$ represents the diffusion capacitance of forward bias of Base - emitter junction

$C_u$ transition capacitance due to reverse bias of collector and Base junction.

The resistance $r_b$ includes the base contact, base bulk and base spreading resistance level. first is due to actual connection to the base. second includes the resistance from the external terminal to active region of the transistor. Last includes the actual resistance with in the active base region.

$$r_\pi = \beta r_e$$

$r_u$ is very large resistance and provides a feedback path from output to i/p

Circuits in the equivalent model. $r_o$ represents the output resistance across the load.

For low to midfrequency analysis the effect of the stray capacitive effects can be ignored due to very high reactance levels associated with each.

$r_b$ is very small can be replaced by short circuit $r_u$ is large it can be ignored for many applications.

Typical data sheet values for hybrid $\pi$ model is

$$r_\pi = \beta r_e$$

$$g_m = \frac{1}{r_e}$$

$$r_o = \frac{1}{h_{oe}}$$

$$h_{re} = \frac{r_\pi}{r_\pi + r_u} \approx \frac{r_\pi}{r_u}$$

CB hybrid parameter in terms of CE hybrid parameters

$$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$$

$$h_{rb} = \frac{h_{ie} h_{oe}}{1+h_{fe}} - h_{re}$$

$$h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$$

$$h_{ob} = \frac{h_{oe}}{1+h_{fe}}$$

CC hybrid parameter in terms of CE hybrid parameters

$$h_{ic} = h_{ie}$$

$$h_{rc} = 1 - h_{re}$$

$$h_{fc} = -(1+h_{fe})$$

$$h_{oc} = h_{oe}.$$

## Assignment Questions

1. Explain and obtain the re-model for CB and CE Configurations
2. Derive an expression for voltage gain, i/p impedance and output impedance of an CE fixed bias using hybrid and re model
3. Derive an expression for voltage gain, i/p impedance and output impedance of an emitter follower amplifier using re model and hybrid parameters.
4. with necessary equivalent circuit diagram obtain the DC bias voltages and currents for a Darlington connection.
5. Explain how h-parameters can be obtained from the static characteristics of the transistor (Explain hybrid equivalent model)
6. using complete hybrid equivalent model for Two port system / transistor derive expressions for $A_I$, $A_V$, $Z_i$, $Z_o$.
7. Derive expression for $Z_i$, $Z_o$, $A_V$, $A_I$ for a voltage divider bias circuit of BJT using hybrid model of BJT.
8. Define h-parameter and hence derive h-parameters model for a CE BJT.
9. A voltage source of negligible internal resistance drives a common collector transistor amplifier. the load resistance is 2500Ω the transistor h-parameters are $h_{ie} = 1000\Omega$, $h_{re} = 1$, $h_{fe} = -50$, $h_{oe} = 25\mu A/V$ determine $A_I$, $A_V$, $Z_i$, $Z_o$
10. For an Emitter follower circuit determine $r_e$, $Z_i$, $Z_o$, $A_V$ with $V_{CC} = 20V$, $R_B = 470K\Omega$, $R_E = 0.56K\Omega$, $C_E = 100\mu F$, $\beta = 120$, $r_o = 40K\Omega$, $C_C = 10\mu F$

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Logarithms: To define the relationship between the variables of a logarithmic function consider the following mathematical equations.

$$a = b^x \qquad x = \log_b a$$

The variables a, b and x are the same in each equation If a is determined by taking the base b to the x power the same x will result if the log of a taken to the base b

For Example Consider if $b = 10$ & $x = 2$

$$a = b^x = 10^2 = 100$$

$$x = \log_b a = \log_{10} 100 = 2.$$

For the electrical/electronics industry and in fact for the vast majority of scientific research the base in the logarithmic equation is chosen as either 10 or the $e = 2.718$

Logarithms taken to the base 10 are referred to as common logarithms where as logarithms taken to the base e are referred to as natural logarithms.

Common logarithm $x = \log_{10} a$

Natural logarithm $y = \log_e a$.

The two are related by the equation $\log_e a = 2.3 \log_{10} a$.

Some properties of common logarithms to any base.

$\log_{10} 1 = 0$

$\log_{10} \frac{a}{b} = \log_{10} a - \log_{10} b$

$\log_{10} \frac{1}{b} = -\log_{10} b$

$\log_{10} ab = \log_{10} a + \log_{10} b.$

**Decibels**: The term decibel has its origin in the fact that power and audio levels are related on a logarithmic basis.

For the standardization the bel (B) is defined by the following equation relating the two power levels $P_1$ and $P_2$.

$$G = \log_{10} \frac{P_2}{P_1} \text{ bel.}$$

The bel was too large unit of measurement for practical purpose so the decibel (dB) is defined such that 10 decibels = 1 bel.

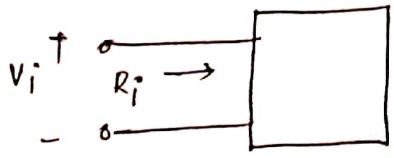
$$G_{dB} = 10 \log_{10} \frac{P_2}{P_1} \text{ dB}.$$

The terminal rating of electronic communication equipment is commonly in decibels. The decibel rating is a measure of the difference in magnitude b/w two power levels for the specified terminal (output) power ($P_2$) there must be reference power level ($P_1$).

The reference level is generally accepted to be 1mW, 6mW standard of earlier is applied. The resistance associated with 1mW power level is 600Ω chosen because it is the characteristic impedance of audio transmission lines

$$G_{dBm} = 10 \log_{10} \frac{P_2}{1mW}\Big|_{600\Omega} \text{ dBm}$$

There exists a second equation for decibels that is applied frequently. It can be described by the following figure.




for $V_i$ equal to some value $V_1$ $P_1 = V_1^2/R$ where $R_i$ is the input resistance of the system

If $V_i$ is increased or decreased to some level $V_2$ then $P_2 = V_2^2/R_i$

$$G_{dB} = 10 \log_{10} \frac{P_2}{P_1}$$

$$= 10 \log \frac{V_2^2/R_i}{V_i^2/R_i}$$

$$\boxed{G_{dB} = 10 \log_{10} (V_2/V_i)^2 \text{ dB}}$$

$$\boxed{G_{dB} = 20 \log_{10} \frac{V_2}{V_i} \text{ dB}}$$

For example the magnitude of the overall voltage gain of a cascaded system is given by

$$|A_{V_T}| = |A_{V_1}| \, |A_{V_2}| \, |A_{V_3}| \cdots |A_{V_n}|$$

Applying the proper logarithmic relationship results in

$$G_V = 20 \log_{10} |A_{V_T}| = 20 \log_{10} |A_{V_1}| + 20 \log_{10} |A_{V_2}| + \cdots 20 \log_{10} |A_{V_n}| \text{ dB}.$$

$$G_{dB_T} = G_{dB_1} + G_{dB_2} + G_{dB_3} + \cdots + G_{dB_n} \text{ dB}$$

Prob: The i/p power to a device is 10,000 W at a voltage of 1000 V the output power is 500 W and output impedance is 20 Ω

① find power gain in decibels

② find the voltage gain in decibels

③

$$G_{dB} = 10 \log_{10} P_o/P_i = 10 \log_{10} \frac{500 \text{ W}}{10 \text{ KW}} = 10 \log_{10} \frac{1}{20} = -10 \log_{10} 20$$

$$= -10 (1.301) = -13.01 \text{ dB}$$

$$G_V = 20 \log_{10} \frac{V_o}{V_i} = 20 \log_{10} \frac{\sqrt{PR}}{1000} = 20 \log_{10} \frac{\sqrt{500 \text{ W} \times 20 \Omega}}{1000 \text{ V}}$$

$$= 20\log_{10}\frac{100}{1000} = 20\log_{10}\frac{1}{10} = -20\log_{10} 10 = -20\,dB$$

$\therefore$

## Frequency response of Amplifier

Frequency response is the plot of Magnitude of Voltage gain as a function of frequency In transistor amplifier the low frequency response is analysed by coupling capacitors and bypass capacitors. The high frequency response is analysed by transistor parastic capacitances & stray wiring capacitance

## General frequency Consideration

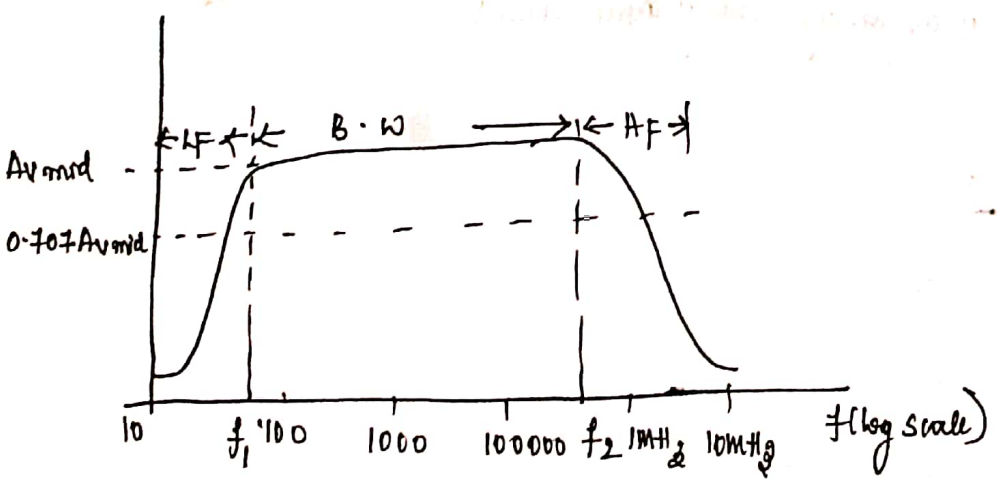
At low frequency → Coupling capacitor & Bypass capacitors effect the signal
At high frequency → Stray wiring capacitance and parastic capacitance effect the signal

## Frequency response of RC Coupled Amplifier

The frequency response of an amplifier is the plot of the magnitude of voltage gain as a function of frequency. Figure below shows the frequency response of RC coupled amplifier

X-axis is frequency (which is usually logarithmic scale to facilitate low frequency to high frequency

Y-axis is magnitude of gain $|A_V|$




Frequency response of RC coupled amplifier.

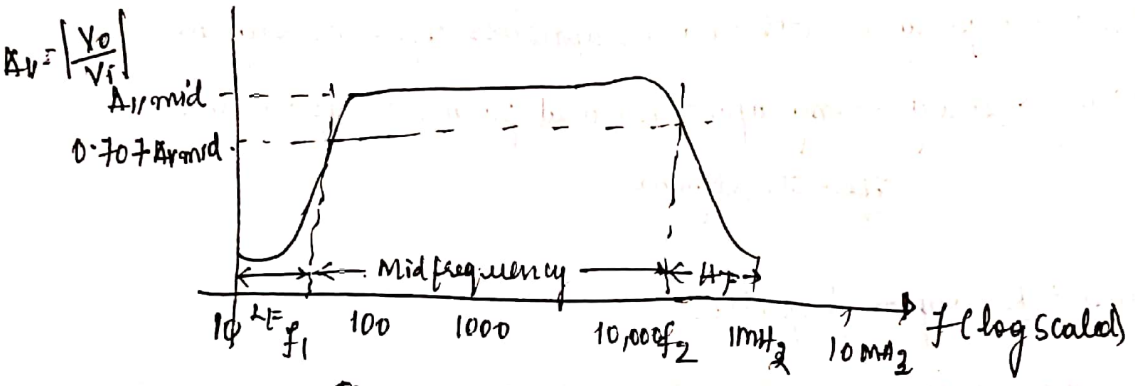
## Frequency response of transformer coupled amplifier.

At low frequencies the gain drops due to small value of $X_L$. At $f=0$

$$X_L = 2\pi f L \quad = \quad X_L = 0$$

Therefore low frequency response is due to small value of $X_L$

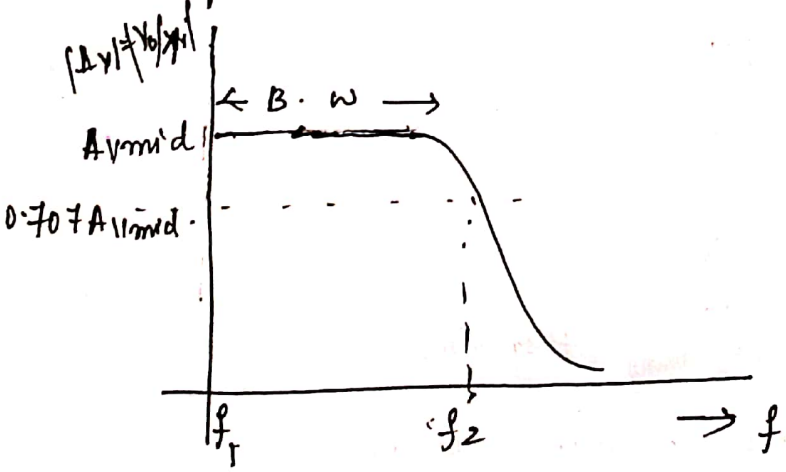
At high frequencies gain drops due to stray capacitance b/w turns of primary and secondary winding




Frequency response of transformer coupled amplifier.

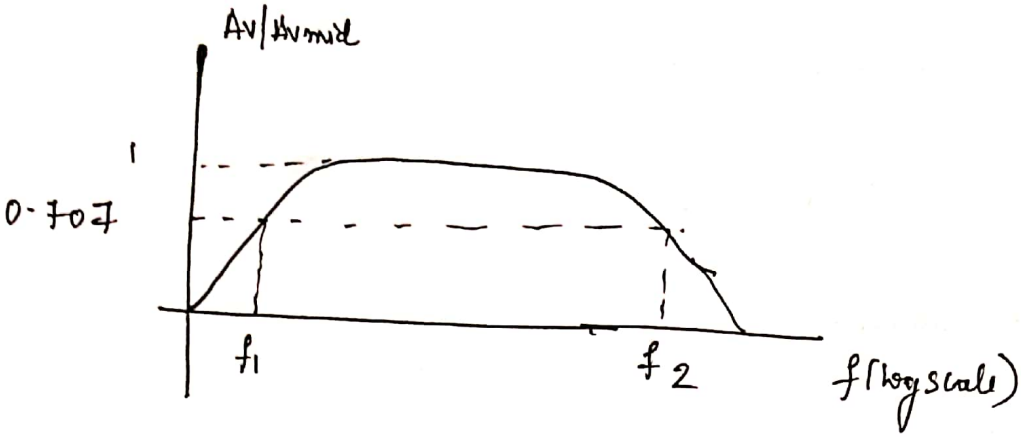
## Frequency response of direct coupled amplifier

Direct coupled amplifier donot use coupling and bypass capacitors As a result there is no drop in gain at low frequencies The frequency response curve is flat upto the upper cutoff frequency Gain drops at high frequences due to the device internal capacitances and the stray wiring capacitances

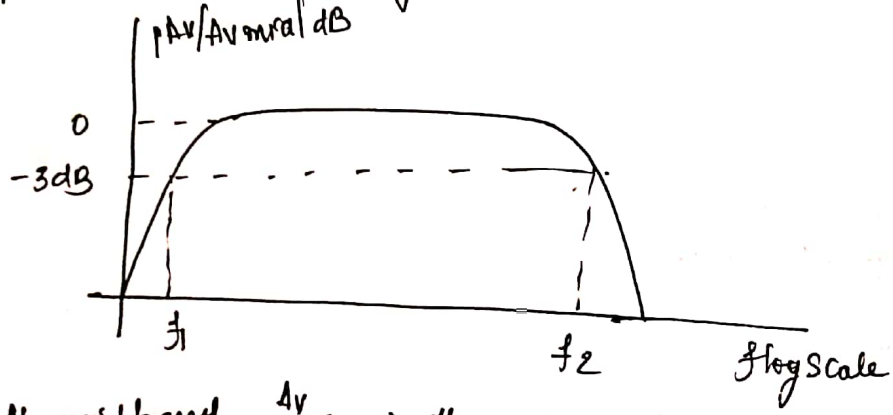


## Normalized gain frequency plot

$$\text{Normalized gain} = \frac{A_v}{A_{vmid}}.$$




In Communication application such as audio and video, it is more useful to represent the normalized gain in dB




At midband $\frac{A_v}{A_{vmid}} \Rightarrow$ the normalized mid band gain is Equal to 1

The normalized gain at cut-off frequencies $\frac{0.707\,A_{vmid}}{A_{vmid}} = 0.707$.

Normalized decibal Vtg gain is $\left.\frac{A_v}{A_{vmid}}\right|_{dB} = 20 \log_{10}\left[\frac{A_v}{A_{vmid}}\right]$

Normalized decibel Vtg gain in mid band is

$$20 \log_{10}\left[\frac{0.707\,A_{vmid}}{A_{vmid}}\right] = -3\,dB$$

## Half power frequencies and Bandwidth

The frequencies $f_1$ and $f_2$ at which the gain is $0.707 A_{vmid}$ are called cutt-off frequencies or corner frequencies or break frequencies $f_1$ is called the lower cutt off frequency and $f_2$ the upper cutt-off frequency.

The bandwidth of the amplifier is given by.

$$B.W = f_2 - f_1$$

The output voltage in the midband is

$$|V_o| = |A_{vmid}||V_i|$$

$$|A_{v(mid)}| = \left|\frac{V_o}{V_i}\right|$$

output power in the midband is

$$P_{o(mid)} = \frac{|V_o|^2}{R}$$

$$\boxed{P_{o(mid)} = \frac{|A_{vmid}|^2 |V_i|^2}{R}}$$

The output voltage at cutt-off frequencies is

$$|V_o| = |0.707 A_{vmid}||V_i|$$

The output power at cutt-off frequencies is

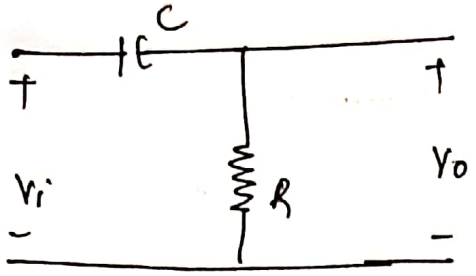
$$\boxed{P_{o(cut-off)} = \frac{|0.707 A_{vmid}|^2 |V_i|^2}{R}}$$

$$P_{o\,cut-off} = \frac{0.5 |A_{vmid}|^2 |V_i|^2}{R_0}$$

$$\boxed{P_{o(cut-off)} = 0.5\, P_{o(mid)}}$$

The o/p power at cutt off frequencies is half the mid band power output for this reason $f_1$ and $f_2$ are also called the half power frequencies.

**Mathematical Analysis** : Consider the ckt as shown below.




By using Vtg divider rule

$$V_o = \frac{V_i R}{R - jX_C} \qquad A_V = \frac{V_o}{V_i}$$

$$\frac{V_o}{V_i} = \frac{R}{R - jX_C}$$

$$A_V = \frac{R}{R\left(1 - j\frac{X_C}{R}\right)}$$

$$A_V = \frac{1}{1 - j\frac{X_C}{R}}$$

$$|A_V| = \frac{1}{\sqrt{1 + \left(\frac{X_C}{R}\right)^2}}$$

At $f = 0$ $\quad X_C = \frac{1}{2\pi f C} = \frac{1}{2\pi(0)C} = \infty$

$$|A_V| = \frac{1}{\sqrt{1+\infty}} = 0$$

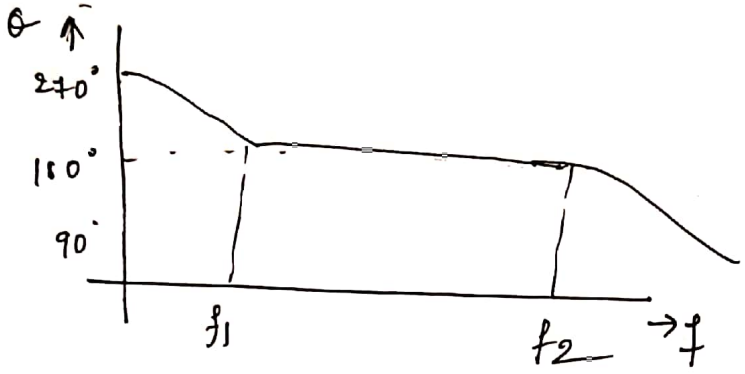
} At low frequency

At $f = \infty$ $\quad X_C = \frac{1}{2\pi f C} = \frac{1}{2\pi(\infty)C} = 0$ $\quad A_V = \frac{1}{\sqrt{1+0}} = 1 = |A_{V(mid)}|$ } At High frequency

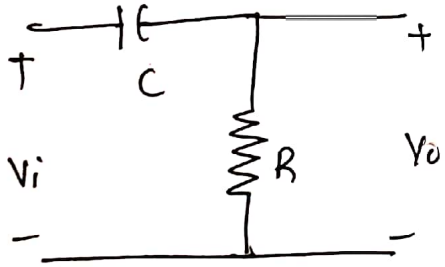
Phase angle plot: A stage RC coupled amplifier introduces a 180° phase shift b/w i/p & o/p signals in the mid band region.

At low frequencies $V_o$ lag $V_i$ - by an additional angle $\theta_1$

At high frequencies $V_o$ leads by $V_i$ - by an additional angle $\theta_2$




Low frequency analysis: In low frequency analysis the response is like a high pass filter as shown in graph. Therefore it can be modeled as high pass filter




Capacitor C - represents combined effect of coupling and bypass capacitors

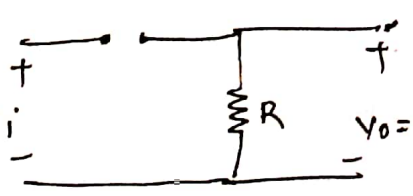
Resistor R → represents combined effect of resistive elements of the amplifier Network

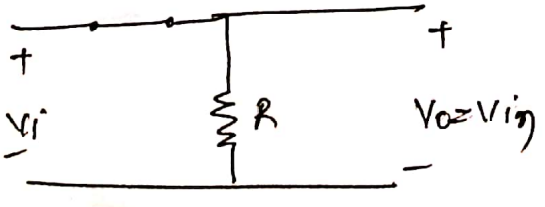
Capacitive reactance

$$X_C = \frac{1}{2\pi f C}$$

At $f=0$, $X_C = \infty\ \Omega$ at low frequencies capacitor acts as open circuit $\therefore V_o = 0$

At $f=\infty$, $X_C = 0\ \Omega$ at high frequencies capacitor acts as short ckt $\therefore V_o = V_{in}$



$|A_V|_{mid}(dB) = 20\log 1 = 0dB$

∴ Midband and high frequency response of coupling & bypass capacitors are same

→ When the capacitive reactance equals to the resistance i.e $X_C = R$

$$|A_V| = \frac{1}{\sqrt{1+\left(\frac{X_C}{R}\right)^2}} = \frac{1}{\sqrt{1+\left(\frac{X_C}{X_C}\right)^2}} = \frac{1}{\sqrt{2}}$$

$$= \frac{1}{\sqrt{2}} \times 1 = \frac{1}{\sqrt{2}}|A_{vmid}|$$

Corresponding magnitude in dB

$$|A_V|_{dB} = 20\log 1/\sqrt{2} = -3dB$$

The above condition is satisfied only for cutt-off frequency

At cutt-off frequency

$$X_C = R$$

$$\frac{1}{2\pi f C} = R$$

$$\boxed{f = \frac{1}{2\pi RC}}$$

$$\boxed{f_1 = \frac{1}{2\pi RC}}$$

where f is lower & upper cutt off frequency denoted by $f_1$

* Let us consider $\frac{X_C}{R} = \frac{1}{2\pi f C R} = \frac{1}{2\pi C R}\cdot\frac{1}{f}$

where f is the general frequency

$$\therefore \frac{X_C}{R} = \left[\frac{f_1}{f}\right]$$

$$|A_V| = \frac{1}{\sqrt{1+\left(\frac{X_C}{R}\right)^2}}$$

$$\therefore = \frac{1}{\sqrt{1+\left(\frac{f_1}{f}\right)^2}}$$

$$\theta_1 = \tan^{-1}\left[\frac{f_1}{f}\right]$$

$\theta_1$ is positive $V_o$ leads $V_i$ by an angle $\theta_1$

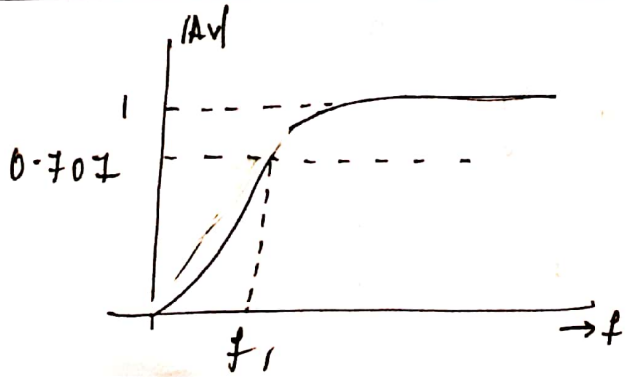
$$A_V = |A_V| \angle \theta_1$$

$$A_V = \frac{1}{\sqrt{1+\left(\frac{f_1}{f}\right)^2}} \quad \angle \tan^{-1} f_1/f$$

## Bode plot of low frequency response

$$|A_V| = \frac{1}{\sqrt{1+\left(\frac{f_1}{f}\right)^2}}$$

$$\text{In dB} = |A_V|_{dB} = -20 \log \sqrt{1+\left(\frac{f_1}{f}\right)^2}$$

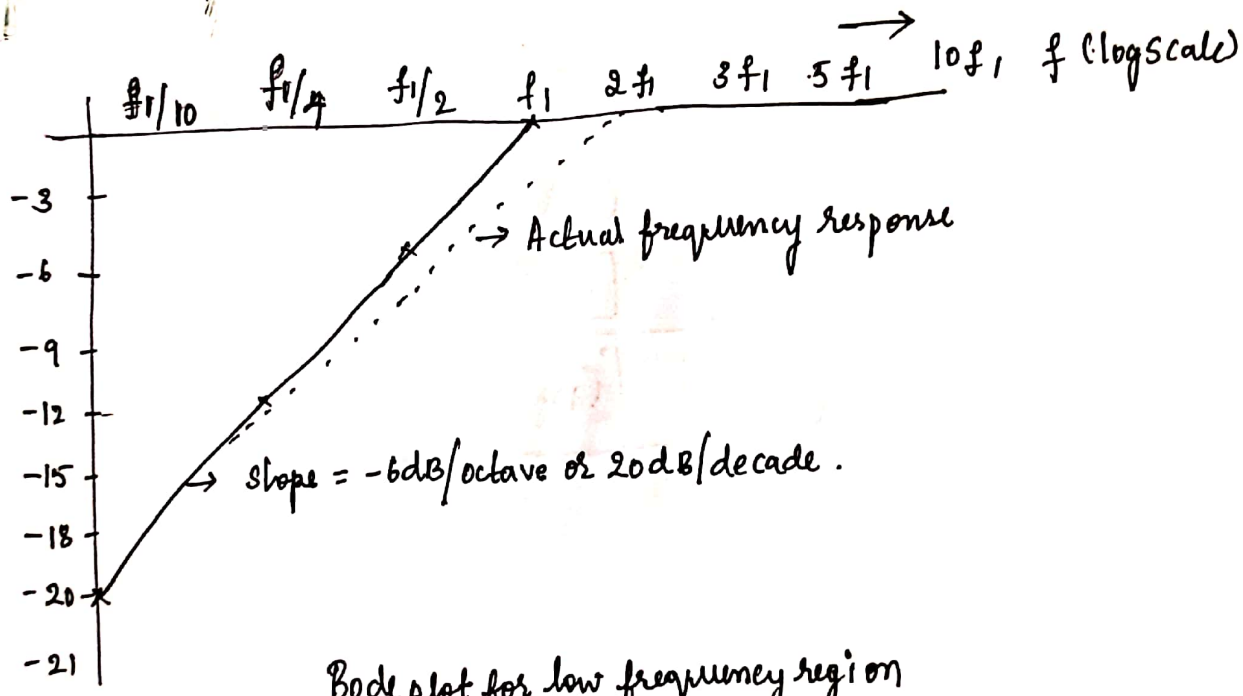



Low frequency response of HPF RC circuit

| $f$ | $f_1/f$ | $A_V = -20\log(f_1/f)$ |
|---|---|---|
| $f_1/10$ | 10 | $-20$ dB |
| $f_1/4$ | 4 | $-12$ dB |
| $f_1/2$ | 2 | $-6$ dB |
| $f_1$ | 1 | 0 dB |

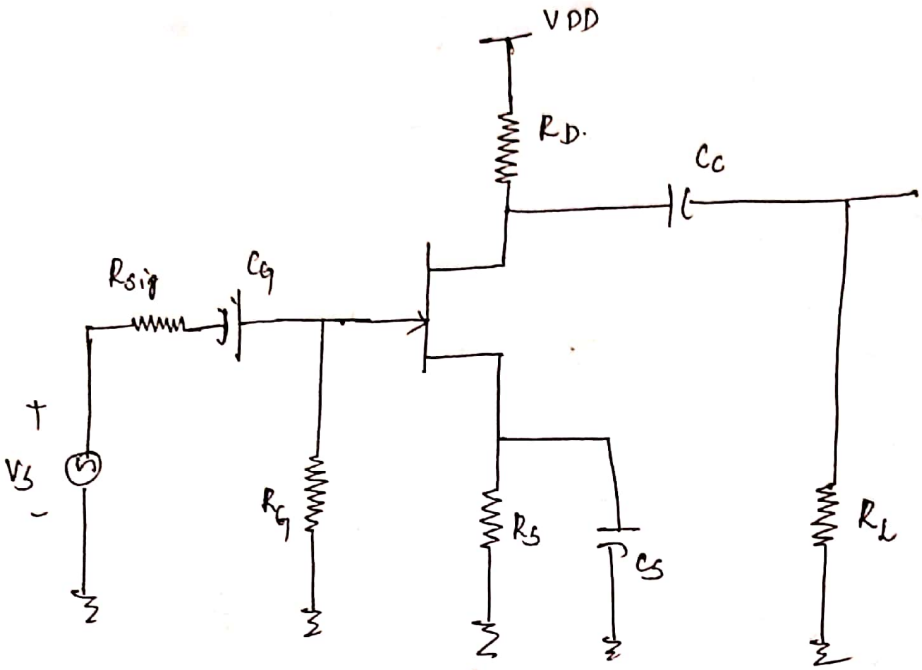
A change in frequency by a factor of two is equal to one octave.

A change in frequency by a factor 10 is equal to one decade.

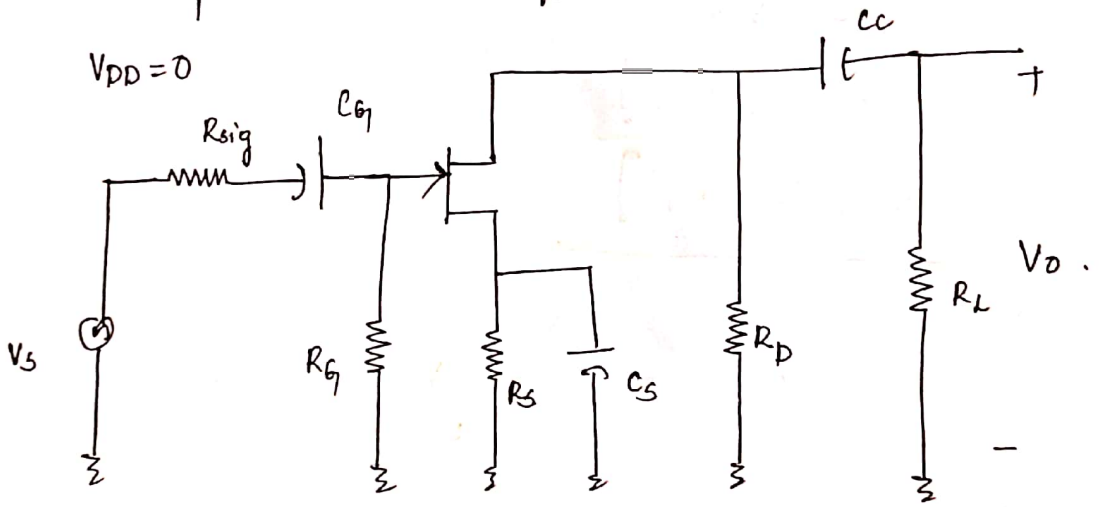



Bode plot for low frequency region

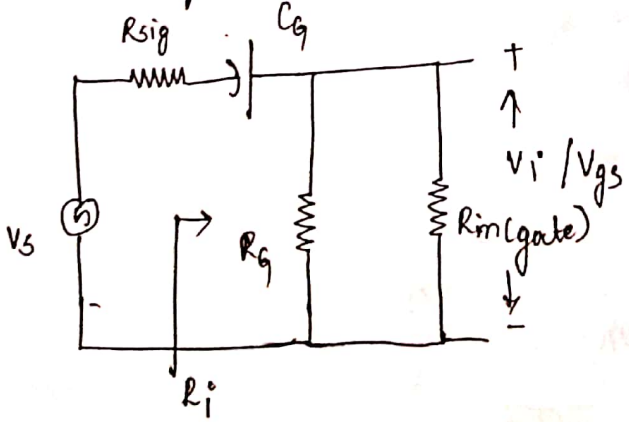
# Low frequency response of FET Amplifier




Capacitive element that affect the low frequency of a JFET amplifier.




Consider the input network




$R_i = R_G \,||\, R_{in(gate)}$.

$\boxed{R_i = R_G}$

$$R_{in(gate)} = \frac{|V_{GS}|}{|I_{GSS}|}$$

$V_{GS}$ = Voltage across gate and Source

$I_{GSS}$ = Gate reverse Current.

$R_G >> R_{sig}$, $R_{in} >> R_{in(gate)}$

Therefore $R_i = R_G$

$$|V_i'| = \frac{|V_s|\, R_i'}{(R_{sig} + R_i') + X_{CG}}$$

$$|V_i'| = \frac{|V_s|\,(R_i'/R_{sig} + R_i')}{1 + \left(\frac{X_{CG}}{R_{sig} + R_i}\right)}$$

for $f = 0$, $X_{CG} = \infty$ and for $f = \infty$, $X_{CG} \to 0$

$$|V_i'| = |V_s|\,(R_i'/R_{sig} + R_i')$$

$$|V_i|_{mid} = |V_s|\,(R_i'/R_{sig} + R_i')$$

Consider $\frac{X_{CG}}{R_{sig} + R_i} = 1$

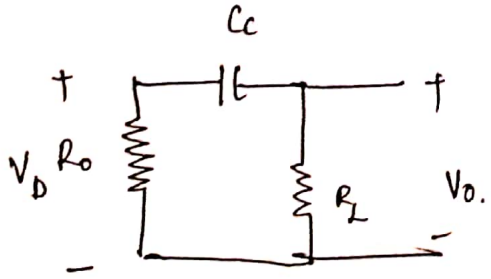
$$X_{CG} = R_{sig} + R_i'$$

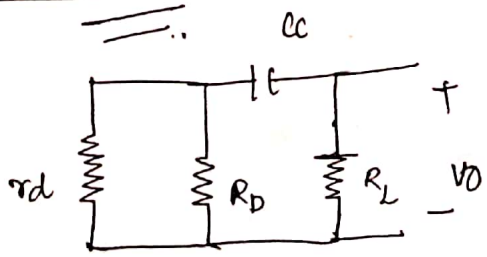
$$\frac{1}{2\pi f C_G} = R_{sig} + R_i'$$

$$f = \frac{1}{2\pi (R_{sig} + R_i)\, C_G}$$

$$\therefore f_{LCG} = \frac{1}{2\pi (R_{sig} + R_i)\, C_G}$$

Similarly consider the output circuit



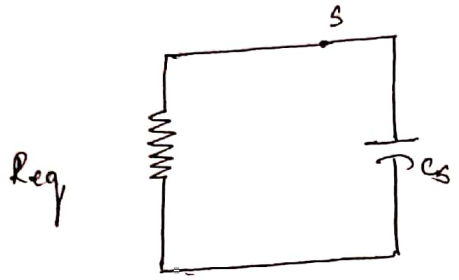

$R_o = r_d \| R_D$

$$V_o = \frac{V_D\,(R_L/R_o + R_L)}{1 + \frac{X_{CG}}{R_o + R_L}}$$

$$f_{L_{CC}} = \frac{1}{2\pi (R_L + R_o) C_C}$$

$$R_o = r_d \| R_D.$$

Consider the ckt as shown below




$R_{eq}$

$$f_{L_{CS}} = \frac{1}{2\pi R_{eq} C_S}$$

$$R_{eq} = \frac{R_S}{1 + \frac{R_S (1 + g_m r_d)}{(r_d + R_D \| R_L)}}$$

if $r_d = \infty \Omega$

$$\boxed{R_{eq} = R_S \| \frac{1}{g_m}}$$

Prob: Determine the lower cutoff frequency of an FET amplifier with the following parameters $C_G = 0.01 \mu F$, $C_C = 0.5 \mu F$, $C_S = 2 \mu F$, $R_{sig} = 10 K\Omega$, $R_G = 1 M\Omega$, $R_D = 4.7 K\Omega$, $R_S = 1 K\Omega$, $R_L = 2.2 K\Omega$, $I_{DSS} = 8 mA$, $V_p = -4 V$, $r_d = \infty \Omega$, $V_{DD} = 20 V$

List of DC Conditions for FET Amplifier.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$V_{GS} = -I_D R_S$$

$V_{GSQ} = -2 V$ and $I_{DQ} = 2 mA$

$$g_{m0} = \frac{2 I_{DSS}}{|V_p|} = \frac{2 \times 8mA}{4V} = 4mS$$

$$g_m = g_{m0}\left(1 - \frac{V_{GSQ}}{V_p}\right)$$

$$g_m = 4mS\left(1 - \frac{+2V}{+4V}\right)$$

$$g_m = 4mS\left(1 - \frac{1}{2}\right) = 2mS$$

$$\boxed{g_m = 2mS}$$

$$f_{LG} = \frac{1}{2\pi (R_{sig} + R_G) C_G} = \frac{1}{2\pi (1M + 10K)\, 0.01\mu F} = 15.8\,Hz$$

$$f_{LC} = \frac{1}{2\pi (R_o + R_L) C_C} = \frac{1}{2\pi (4.7K + 2.2K)\, 0.5\mu F} = 46.13\,Hz$$

$$R_o = r_d \| R_D = R_D$$

$$R_{eq} = R_S \| \frac{1}{g_m} = 1K\Omega \| \frac{1}{2mS} = 333.33\Omega$$

$$f_{LS} = \frac{1}{2\pi R_{eq} C_S} = \frac{1}{2\pi \times 333.33\Omega \times 2\mu F}$$

$$\boxed{f_{LS} = 238.73\,Hz}$$

Midband gain of the System determined by

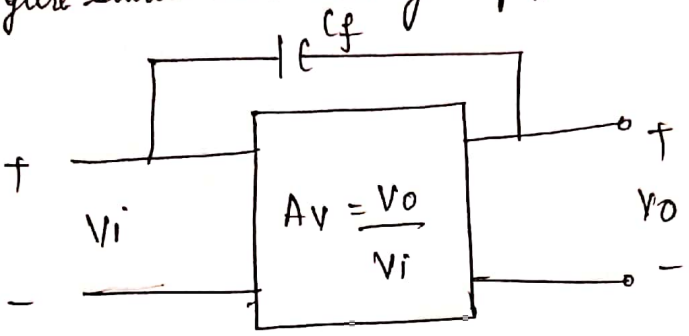
$$A_{V(mid)} = \frac{V_o}{V_i} = -g_m (R_D \| R_L)$$

$$= -2mS (4.7K \| 2.2K)$$

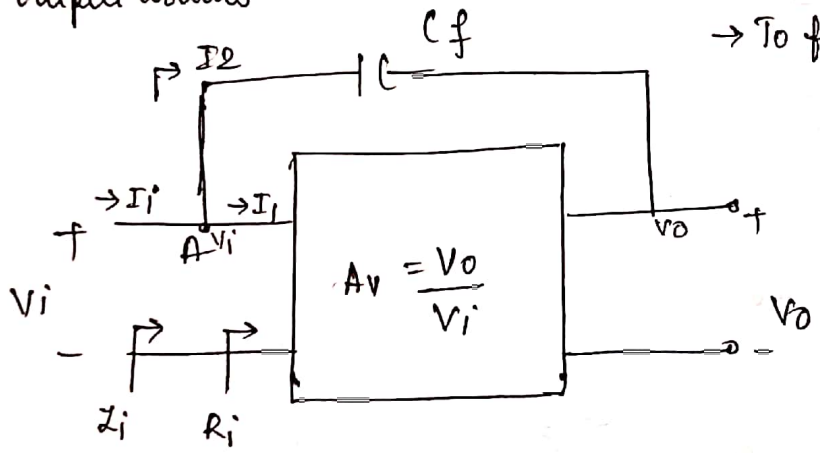
$$\boxed{A_{V(mid)} = -3}$$

## Miller Effect Capacitance

Figure shows the inverting amplifier with capacitance Cf b/w input & output nodes.




Gain ($A_V$) is negative for inverting amplifier since Vo and Vi are 180° out of phase using miller theorem we can find the loading effect of Cf on the input and output circuits.




→ To find miller i/p capacitance (CMi)

$$R_i = \frac{V_i}{I_i} \Rightarrow I_i = \frac{V_i}{R_i}$$

$$Z_i = \frac{V_i}{I_i'} \Rightarrow I_i' = \frac{V_i}{Z_i}$$

Applying KCL at node A.

$$I_i' = I_1 + I_2$$

$$\frac{V_i}{Z_i'} = \frac{V_i}{R_i'} + \frac{V_i - V_o}{X_{cf}}$$

$$A_v = \frac{V_o}{V_i}$$

$$V_o = A_V V_i$$

$$\frac{V_i}{Z_i} \quad \frac{-V_i}{R_i} + \frac{V_i - A_V V_i}{X_{cf}}$$

$$\frac{V_i}{Z_i} = \frac{V_i}{R_i} + V_i \frac{(1 - A_V)}{X_{cf}}$$

$$\frac{1}{Z_i'} = \frac{1}{R_i} + \frac{(1 - A_V)}{C_f}$$

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1 - A_V}{X_{cf}}$$

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{\frac{X_{cf}}{1 - A_V}}$$

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{CM_i}}$$

Let $\boxed{X_{CM_i} = \frac{X_{cf}}{1 - A_V}}$ → (1)

$$X_{cf} = \frac{1}{2\pi f C_f}$$

$$\boxed{X_{CM_i} = \frac{1}{2\pi f C_{M_i}}} \rightarrow (2)$$

$C_{M_i}$ - Input miller capacitance

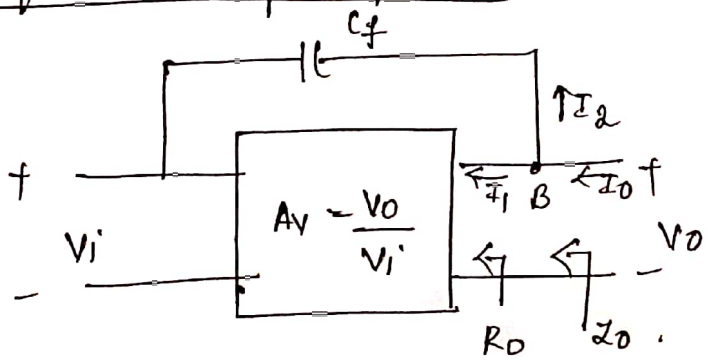
$$X_{CM_i} = \frac{X_{cf}}{1 - A_V}$$

$$\boxed{X_{CM_i} = \frac{1}{2\pi f (1 - A_V) C_f}} \rightarrow (3)$$

equating Eqn (2) & (3) we get

$$\boxed{C_{M_i} = (1 - A_V) C_f}$$

To find miller output capacitance



Applying KCL at node B.

$$I_0 = I_1 + I_2$$

$$\frac{V_o}{Z_o} = \frac{V_o}{R_o} + \frac{V_o - V_i}{X_{cf}}$$

$$\frac{V_o}{Z_o} = \frac{V_o}{R_o} + \frac{1 - V_i/V_o}{X_{cf}}$$

$$A_v = \frac{V_o}{V_i} \qquad 1/A_v = \frac{V_o}{V_i}$$

$$\frac{1}{Z_o} = \frac{1}{R_o} + \frac{1 - 1/A_v}{X_{cf}}$$

$$\frac{1}{Z_o} = \frac{1}{R_o} + \frac{1}{X_{cf}/1 - 1/A_v}$$

$$\text{Let } X_{CM_o} = \frac{X_{cf}}{1 - 1/A_v}$$

$$\frac{1}{Z_o} = \frac{1}{R_o} + \frac{1}{X_{CM_o}}$$

$$X_{cf} = \frac{1}{2\pi f C_f}$$

$$X_{CM_o} = \frac{1}{2\pi f C_{M_o}} = \frac{1}{2\pi f C_f (1 - 1/A_v)}$$

$$\boxed{C_{M_o} = C_f (1 - 1/A_v)}$$

which is called as miller o/p capacitance

Conclusion: A capacitance b/w i/p & o/p nodes of an inverting amplifier can be replaced by

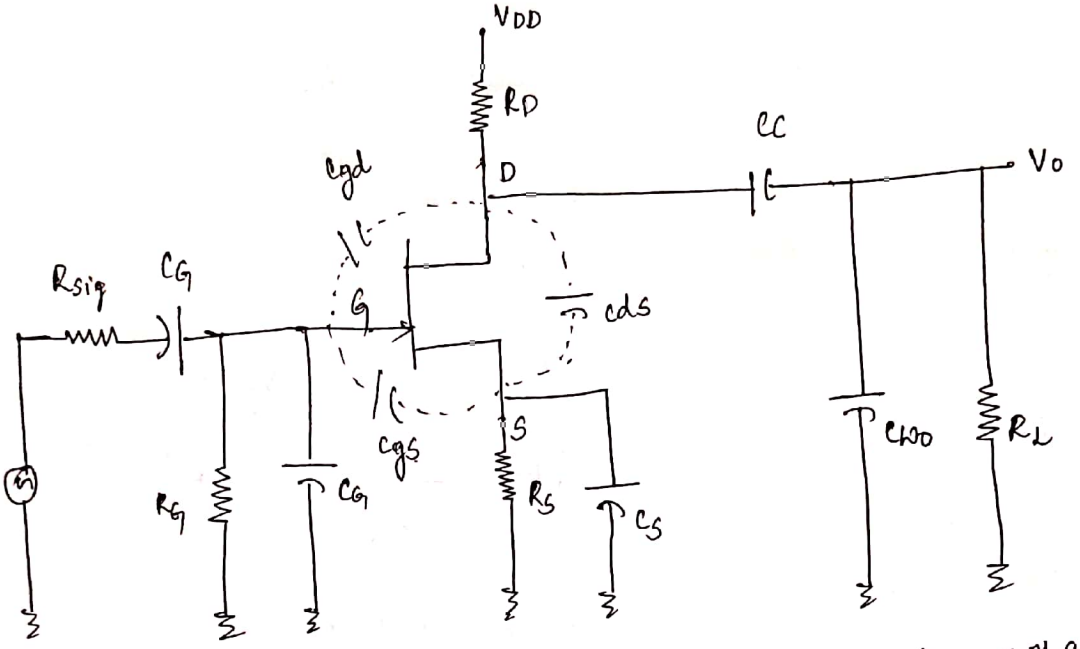
$C_{M_i}$ = Miller input capacitance $(1 - A_v) C_f$ b/w i/p & ground

$C_{M_o}$ = Miller output capacitance $C_f (1 - 1/A_v)$ b/w o/p & ground.

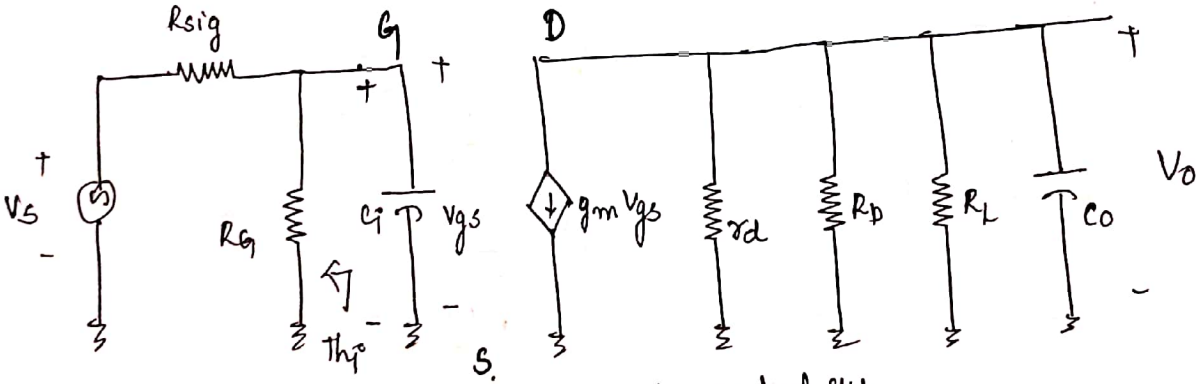
If Amplifier is non-inverting replace sign by positive.

## High frequency response - BJT Amplifier

At the high frequency end there are two factors that define the -3dB cutoff point the network capacitance (parasitic and wiring) and frequency dependence of $h_{fe}(\beta)$.

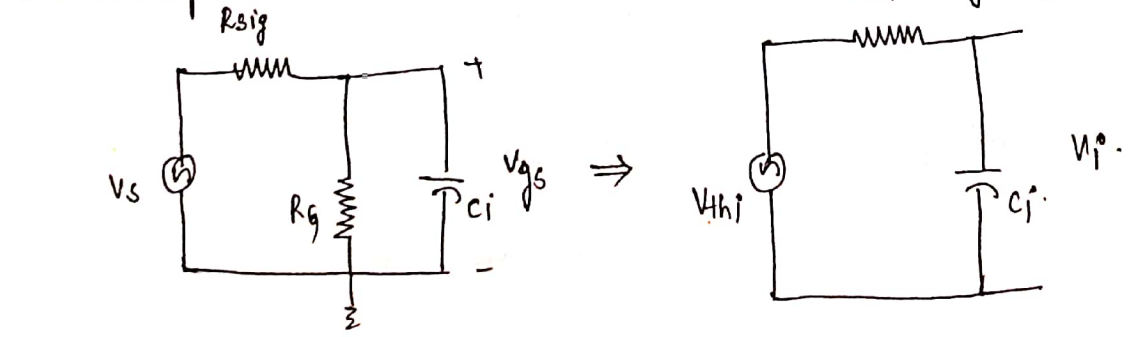



Capacitive elements that affect the high frequency response of a JFET amplifier -

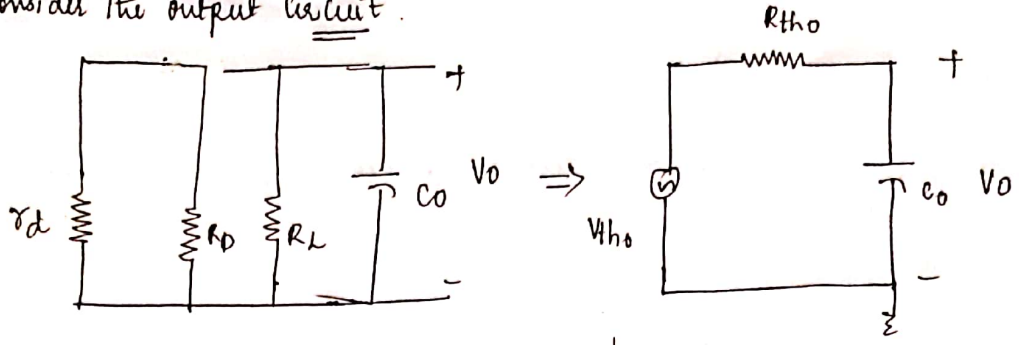



High frequency ac Equivalent ckt.

Consider the input circuit



Consider the output circuit.




$$R_{tho} = R_D \| R_L \| r_d$$

From the input circuit we have

$$V_i^\circ = \frac{V_{thi}^\circ \times C_i}{R_{thi} + X_{C_i}^\circ}$$

$$V_i^\circ = \frac{V_{thi} \times C_i^\circ}{\left(\frac{R_{th}}{X_{C_i}} + 1\right) X_{C_i}}$$

$$|V_i^\circ| = \frac{|V_{thi}|}{\sqrt{1 + \left(\frac{R_{thi}}{X_{C_i}}\right)^2}} \rightarrow (1)$$

$f = \infty$, $X_{C_i}^\circ = 0$ and $f = 0$, $X_{C_i}^\circ = \infty$ on

Substituting this condition

Eq (1) becomes $|V_{thi}^\circ| = |V_s|$ i.e $|V_{thi}|_{Mid} = |V_s|$

Consider $\frac{R_{thi}}{X_{C_i}^\circ} = 1$

$$X_{C_i}^\circ = R_{thi}^\circ$$

$$f_{Hi}^\circ = \frac{1}{2\pi R_{thi} C_i^\circ}$$

$$C_i = C_{Wi}^\circ + C_{gs} + C_{Mi}^\circ$$

$$C_{Mi}^\circ = (1 - A_V) C_f$$

$$\boxed{C_{Mi} = (1 - A_V) C_{gd}}$$

$$A_V = -g_m (R_D \| R_L)$$

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_{mo} = \frac{2 I_{DSS}}{|V_P|}$$

$\boxed{V_{GS} = -2V}$

From the output CKT

$$V_o = \frac{V_{tho} X_{Co}}{R_{tho} + X_{Co}}$$

$$V_o = \frac{V_{tho} X_{C_o}}{\left(\frac{R_{tho}}{X_{Co}} + 1\right) X_{C_o}}$$

$$|V_o| = \frac{|V_{tho}|}{\sqrt{\left(\frac{R_{tho}}{X_o}\right)^2 + 1}} \rightarrow (2)$$

$f = \infty$, $X_{C_i}^\circ = 0$ & $f = 0$, $X_{C_i}^\circ = \infty$ on Substituting in (2) we get $|V_o| = |V_{tho}|$ i.e $|V_o|_{Mid} = |V_{tho}|$

Consider $\frac{R_{tho}}{X_{Co}} = 1$

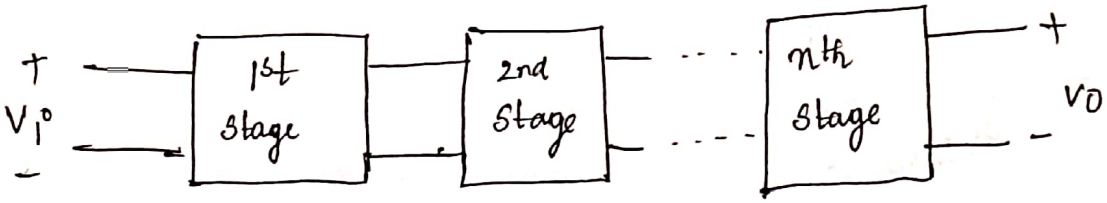
$$f_{Ho} = \frac{1}{2\pi R_{tho} C_o}$$

$$C_o = C_{Wo} + C_{ds} + C_{Mo}$$

$$C_{Mo} = (1 - 1/A_V) C_{gd}$$

## Multistage frequency effects

Assuming identical n-stages of amplifiers connected in cascaded as shown in fig Let the mid band gain of each of the stages be $A_{V(mid)}$




Cascaded connection of n number of RC-coupled amplifiers.

For the low frequency the overall voltage gain is given by

$$A_{V(low)overall} = A_{V_1(low)} \times A_{V_2(low)} \cdots A_{Vn\,low}$$

Since all the stage are identical.

$$A_{V_1(low)} = A_{V_2(low)} = A_{V(3)low} = A_{V(n)low}.$$

$$A_{V(low)overall} = \left[A_{V_1(low)}\right]^n$$

The low frequency gain $A_{V(low)}$ for one stage is given

$$|A_{V(low)}| = \frac{|A_{V(mid)}|}{\sqrt{1+(f_1/f)^2}}$$

$$\left|\frac{A_{V(low)}}{A_{V(mid)}}\right| = \frac{1}{\sqrt{1+(f_1/f)^2}}$$

For n-stage in cascade connection we have

$$\left|\frac{A_{V(low)}}{A_{V(mid)}}\right|^n = \left[\frac{1}{\sqrt{1+(f_1/f)^2}}\right]^n \rightarrow (1)$$

$$\left\{ \frac{|A_{V(low)}|}{|A_{V(mid)}|} \right\}^{n}_{f=f_{L(n)}} = \frac{1}{\sqrt{2}}$$

Eq (1) becomes.

$$\frac{1}{\sqrt{2}} = \left[ \frac{1}{1+(f_1/f_{L(n)})^2} \right]^n$$

$$\sqrt{2} = \left[ \sqrt{1+(f_1/f_{Ln})^2} \right]^n$$

Squaring on both the sides

$$2 = \left[ 1+(f_1/f_{Ln})^2 \right]^n$$

taking $n^{th}$ root on both sides

$$2^{1/n} = \left[ 1+(f_1/f_{L(n)})^2 \right]^{n/n}$$

$$2^{1/n} = 1+\left(\frac{f_1}{f_{L(n)}}\right)^2$$

$$2^{1/n}-1 = \left(\frac{f_1}{f_{L(n)}}\right)^2$$

$$\frac{f_1}{f_{Ln}} = \sqrt{2^{1/n}-1}$$

$$\boxed{f_{L(n)} = \frac{f_1}{\sqrt{2^{1/n}-1}}}$$

$f_{L(n)}$ → Lower 3dB frequency of identical cascaded stages.

$f_1$ = lower 3dB frequency of single stage

$n$ – no of stages.

## overall high frequency cut-off frequency of multistage amplifier

$$\left\{\frac{|A_{V(high)}|}{|A_{V(mid)}|}\right\}^n \leq \left[\frac{1}{\sqrt{1+(f/f_2)^2}}\right]^n \rightarrow (1)$$

Let $f_{H(n)}$ be the upper frequency of the amplifier having n-stage. then at this frequency $f_{H(n)}$ we have.

$$\left\{\frac{|A_{V(high)}|}{|A_{V(mid)}|}\right\}^n = \frac{1}{\sqrt{2}}$$ equation (1) becomes.

$$\frac{1}{\sqrt{2}} = \left\{\frac{1}{\sqrt{1+\left(\frac{f_{H(n)}}{f_2}\right)^2}}\right\}^n$$

$$\sqrt{2} = \left\{\sqrt{1+\left(\frac{f_{H(n)}}{f_2}\right)^2}\right\}^n$$

Squaring & taking nth root

$$2^{1/n} = \left\{1+\left(\frac{f_{H(n)}}{f_2}\right)^2\right\}^{n/n}$$

$$\left(\frac{f_{H(n)}}{f_2}\right)^2 = 2^{1/n}-1$$

$$\frac{f_{H(n)}}{f_2} = \sqrt{2^{1/n}-1}$$

$$\boxed{f_{H_n} = f_2\sqrt{2^{1/n}-1}}$$

Module -2 **FET Small Signal Model** Chapter - 2

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The Ac analysis of an FET Configuration requires that a small signal ac model for the FET to be developed.

An ac voltage applied to the input gate to Source terminal will Control the level of current from drain to Source

Gate to Source voltage Controls the drain to Source Current of an FET

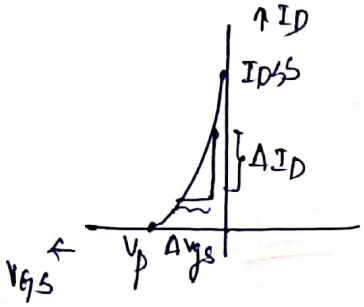
The dc $V_{GS}$ Controls the level of dc drain Current through a relationship known as Shockleys equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

The change in gate to Source voltage Can be determined using the transConductance factor $g_m$ in the following manner

$$\Delta I_D = g_m \Delta V_{gs}$$

$$g_m = \frac{\Delta I_D}{\Delta V_{gs}}$$




Definition of $g_m$ using transfer characteristics

$$g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}}.$$

Mathematical definition of $g_m$

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2\right]$$

$$g_m = I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_p}\right)$$

$$g_m = 2I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)\left(\frac{d}{dV_{GS}}(1)-\frac{1}{V_p}\frac{dV_{GS}}{dV_{GS}}\right)$$

$$g_m = 2I_{DSS}\left[1-\frac{V_{GS}}{V_p}\right]\left[0-\frac{1}{V_p}\right]$$

$$\boxed{g_m = \frac{2I_{DSS}}{|V_p|}\left[1-\frac{V_{GS}}{V_p}\right]}$$

If $V_{GS}=0V$

$$\boxed{\therefore g_{m0} = \frac{2I_{DSS}}{|V_p|}}$$

$$\boxed{\therefore g_m = g_{m0}\left(1-\frac{V_{GS}}{V_p}\right)}$$

**FET i/p impedance** : Input impedance of all the FET's is sufficiently large to assume that the i/p terminals approximate an open circuit in equation form.

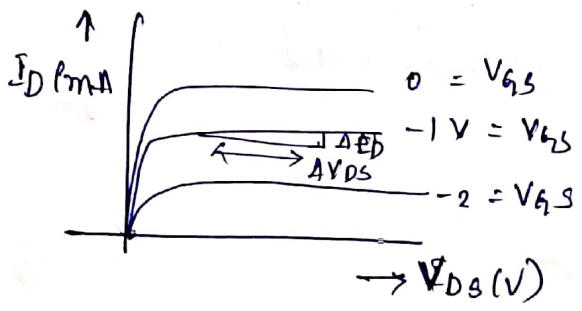
$$\boxed{Z_i = \infty\,\Omega}$$

It is typically practical value of $10^9\Omega = 1000M\Omega$

**FET o/p impedance** : Output impedance of FET's are $Z_o = r_d = 1/Y_{os}$

$Y_{os}$ = 4s (units) is parameter component of an admittance equivalent circuit

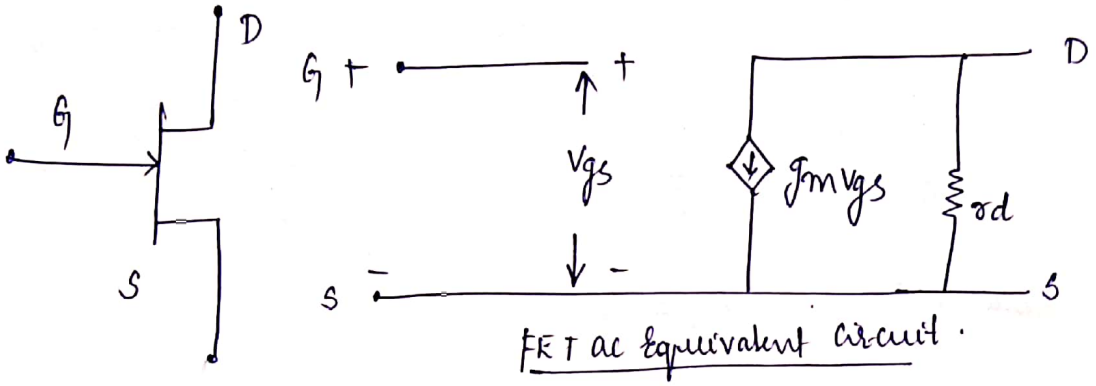
$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}=\text{Constant}}$$



## FET AC Equivalent Circuit (Small Signal Model of FET) (2)

A model for the FET transistor in the ac domain can be constructed the control of $I_d$ by $V_{gs}$ is included as a current source $V_{gs} g_m$ connected from drain to source.

The current source has its arrow pointing from drain to source to establish a 180° phase shift b/w output and input voltages as will occur in actual operation.



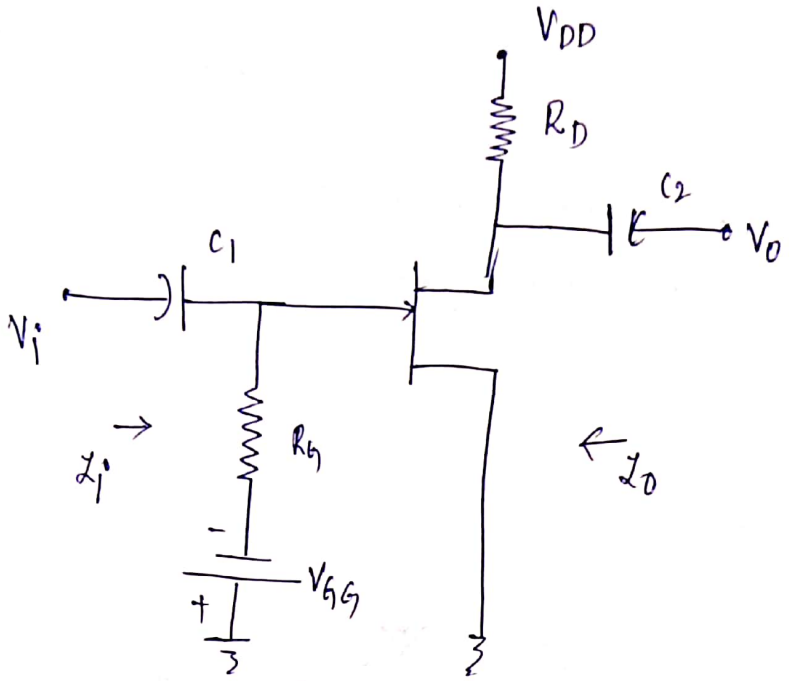

FET ac Equivalent Circuit.

The i/p impedance is represented by the open-circuit at the i/p terminals and the output impedance by resistor $r_d$ from drain to source. Source is common to both input and output circuits whereas gate and drain terminals are only in touch through the controlled current source $g_m V_{gs}$ $r_d$ is ignored. The equivalent circuit is simply a current source whose magnitude is controlled by the signal $V_{gs}$ and parameter $g_m$. (Clearly voltage controlled device).

### Configurations

JFET fixed bias configuration
JFET self bias configuration
JFET Voltage divider bias configuration)
JFET Source follower (Common drain) Configuration
JFET common gate configuration.

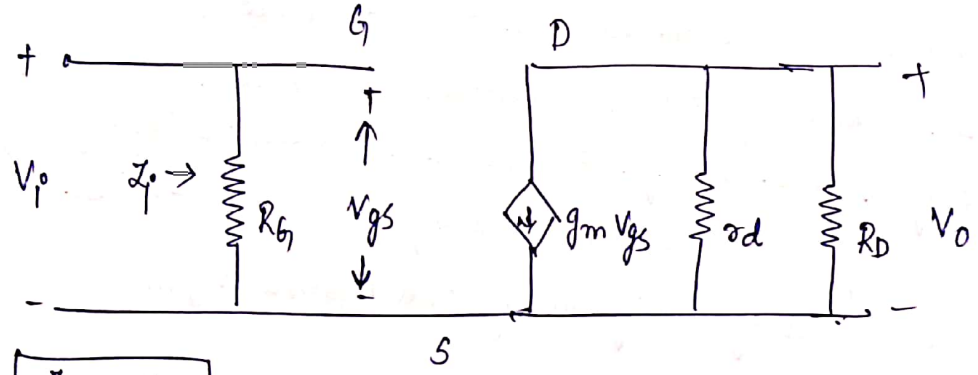
## JFET fixed bias configuration




The fixed bias configuration the coupling capacitors $C_1$ & $C_2$ which isolate the dc biasing arrangement from applied signal and load. They act as short circuit equivalents for the Ac analysis.

Assume $V_{GG} = 0V$, $V_{DD} = 0V$.

## Ac equivalent circuit

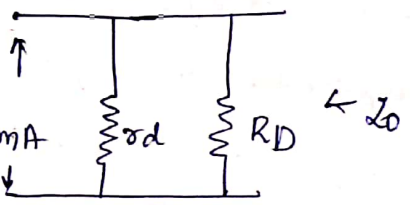



$$Z_i = R_G$$

$Z_o$, $V_i = 0V$, $V_{gs} = 0V$, $g_m V_{gs} = 0mA$

The output impedance

$$Z_o = R_D \| r_d$$




If the resistance $r_d$ is sufficiently large compared to $R_D$ the Approximation

$r_d \| R_D \overset{\eta}{=} R_D$

$\boxed{Z_o = R_D}$ $\quad r_d \geq 10 R_D$

$$A_V = \frac{V_o}{V_i}$$

$V_o = -I_o R_L$

$V_o = -g_m V_{gs} (r_d \| R_D)$ $\qquad V_{gs} = V_i$

$V_o = -g_m V_i (r_d \| R_D)$

$$\frac{V_o}{V_i} = -g_m (r_d \| R_D)$$

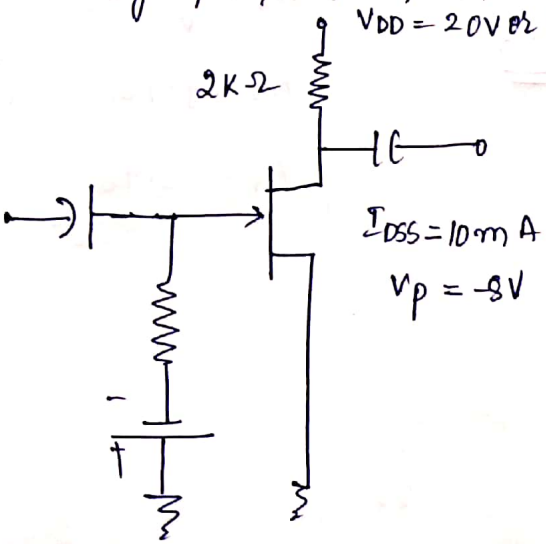
$\boxed{A_V = -g_m (r_d \| R_D)}$

$r_d \geq 10 R_D$

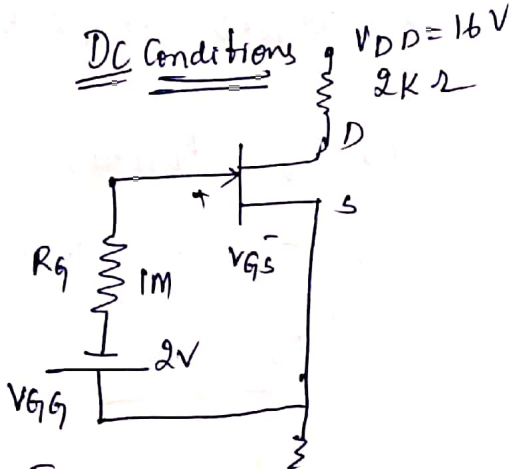
$\boxed{A_V = -g_m R_D}$

Problem: For fixed bias configuration had an operating point defined by $V_{GS(Q)} = -2V$ & $I_{DQ} = 5.625mA$ with $I_{DSS} = 10mA$, $V_p = -8V$, $y_{os} = 40\mu S$

Determine $g_m, r_d, Z_i, Z_o, A_V$, determine $A_V$ by ignoring $r_d$.




DC Conditions




$I_G = 0A$, $R_G = 0\Omega$, Sht Ckt $R_G$

$-V_{GG} - V_{GS} = 0$ .

$V_{GSQ} = -V_{GG} = -2V$

$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2$

$= 10mA\left(1 - \frac{+2V}{+8V}\right)$

$= 10mA\,(1-0.25)^2 = 10mA \times (0.75)^2 = 5.625mA$

$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$

$= 2.5ms\left(1 - \frac{+2V}{+8}\right)$

$\boxed{g_m = 1.88ms}$

$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2 \times 10mA}{8V} = 2.5ms$

$r_d = 1/Y_{OS} = 1/40\mu S = 25K\Omega$

$Z_i = R_G = 1M\Omega$

$Z_o = r_d \| R_D = 2K \| 25K = 1.85K$

$A_V = -g_m (R_D \| r_d)$

$A_V = -1.88ms\,(2K \| 25K)$

$\boxed{A_V = -3.48}$

without $r_d$

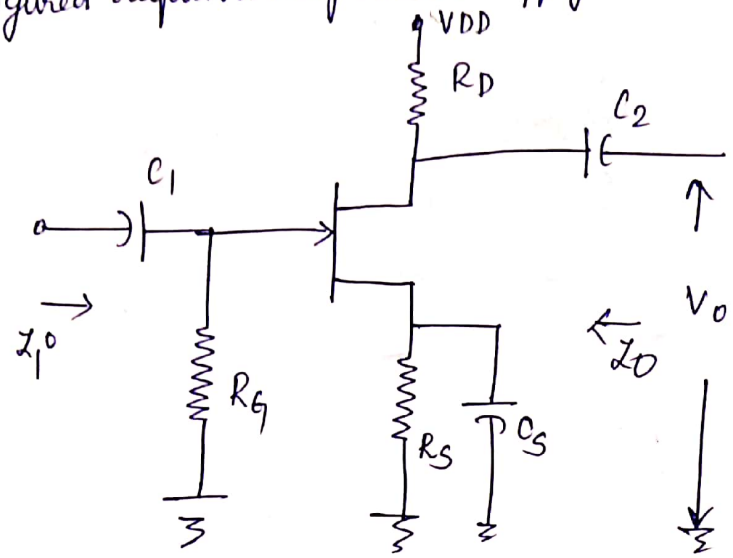
$A_V = -g_m R_D$

$A_V = (-1.88ms)(2K)$

$\boxed{A_V = -3.76}$

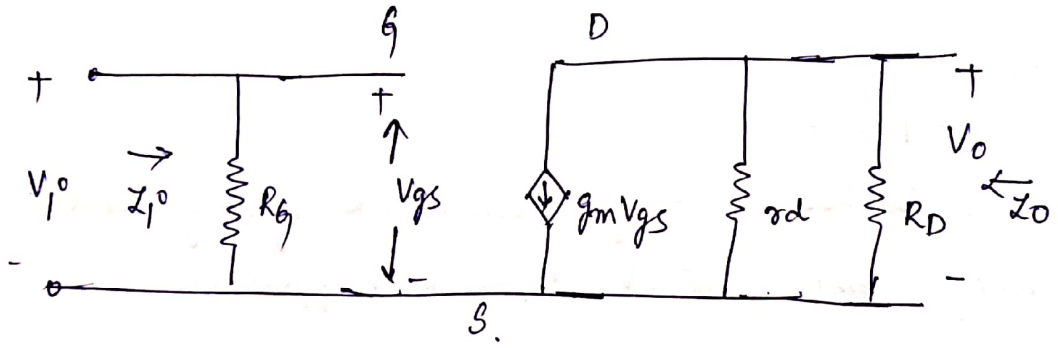
## Self Bias Configuration (Bypassed $R_S$) (Neglecting $R_S$) & $f$.

Fixed bias requires 2 dc sources i.e disadvantage therefore self bias is configured requires only one dc supply.




**AC Equivalent ckt** : Neglect all the dc sources & $C_1$, $C_2$, $C_S$ are Sht ckted

Neglect the effect of $R_S$.




**Input impedance** : $Z_i = R_G$

**output impedance** : $Z_o = R_D \| r_d$

$$\boxed{Z_o = R_D} \quad r_d \geq 10 R_D$$

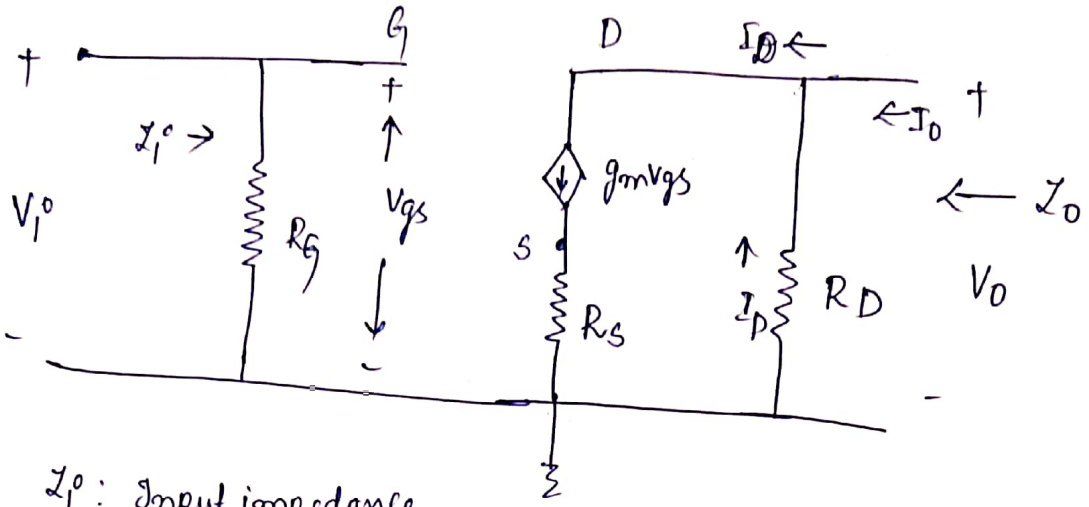
**$A_V$: Gain** : $A_V = \frac{V_o}{V_i^o}$

$V_o = -I_o R_L = -g_m V_{gs} (R_D \| r_d)$

$V_{gs} = V_i^o \quad = -g_m V_i^o (R_D \| r_d)$

$$\boxed{A_V = \frac{V_o}{V_i^o} = g_m (R_D \| r_d)}$$

## Unbypassed RS : Consider the Effect of RS (neglected)




$Z_i^o$ : Input impedance

$$\boxed{Z_i^o = R_G}$$

$Z_o$ : output impedance is defined by

$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i = 0}$$

$V_i^o = 0V$ in the ckt results in the gate terminal being at ground potential. The voltage across $R_G$ is then 0V & $R_G$ has been Effectively shorted out

Apply KCL across output loop

$$I_o + I_D = g_m V_{gs}$$

$$\boxed{V_{gs} = -(I_o + I_D) R_S}$$

$$I_o + I_D = -g_m (I_o + I_D) R_S$$

$$I_o + I_D = -g_m I_o R_S - g_m I_D R_S$$

$$I_o + g_m I_o R_S = -I_D - g_m I_D R_S$$

$$I_o (1 + g_m R_S) = -I_D (1 + g_m R_S)$$

$$\boxed{I_o = -I_D}$$

The controlled current source $g_m V_{gs} = 0A$ for the applied conditions

$V_o = -I_D R_D$

$V_o = -(-I_o) R_D$

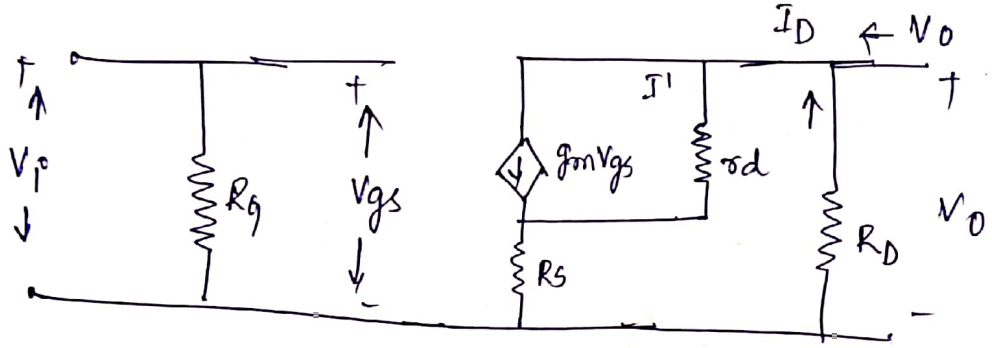
$V_o = -I_o R_D$

$\frac{V_o}{I_o} = R_D$

$$\boxed{Z_o = R_D}$$

$$\boxed{Z_o = \frac{V_o}{I_o} = R_D}$$ $r_d = \infty \Omega$

## $A_V$ Gain for Self Bias Configuration




KVL across the ckt

$V_i - V_{gs} - V_{R_S} = 0$

$V_{gs} = V_i - V_{R_S}$

$$\boxed{V_{gs} = V_i - I_D R_S} \rightarrow (1)$$

KCL across the o/p loop

$I_D = g_m V_{gs} + I'$

Consider voltage across $r_d$

$V_{rd} = V_o - V_{R_S}$

$I' = \frac{V_{rd}}{r_d} = \frac{V_o - V_{R_S}}{r_d}$

$$I_D = g_m V_{gs} + \frac{V_o - V_{RS}}{r_d}$$

$$I_D = g_m (V_i^o - I_D R_S) + \frac{V_o - V_{RS}}{r_d}$$

$$I_D = g_m V_i^o - g_m I_D R_S + \frac{(-I_D R_D) - I_D R_S}{r_d}$$

$$I_D + g_m I_D R_S + \frac{I_D R_D + I_D R_S}{r_d} = g_m V_i^o .$$

$$I_D \left(1 + g_m R_S + \frac{R_D + R_S}{r_d}\right) = g_m V_i^o$$

$$\boxed{I_D = \frac{g_m V_i^o}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}}$$

output voltage

$$V_o = - I_D R_D$$

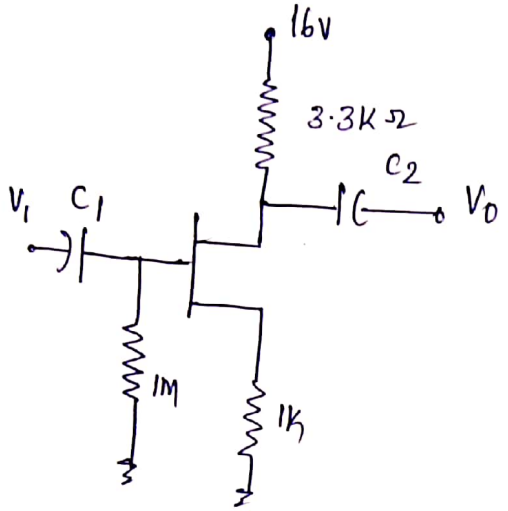
$$V_o = - \frac{g_m V_i^o R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

$$\frac{V_o}{V_i^o} = \frac{-g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

$$\boxed{A_V = \frac{-g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}}$$

## problem on self bias Configuration

For a self bias configuration has an operating point defined by $V_{GS(Q)} = -2.6V$ and $I_{DQ} = 2.6mA$, with $I_{DSS} = 8mA$, $V_P = -6V$, $y_{os} = 20\mu S$ determine $g_m$, $r_d$, $Z_i$, $Z_o$ with & without $r_d$, $A_V$ with and without $r_d$.




$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_{m0} = \frac{2 \times 8mA}{6} = \frac{16m}{6} = 2.66mS$$

$$g_m = g_{m0}\left(1 - \frac{V_{GSQ}}{V_P}\right)$$

$$= 2.66mS\left(1 - \frac{-2.6V}{-6V}\right)$$

$$\boxed{g_m = 1.51mS}$$

$$r_d = \frac{1}{y_{os}} = \frac{1}{20\mu S} = 50K\Omega$$

$$Z_i = R_G = 1M\Omega$$

$$Z_o = R_D = 3.3K\Omega$$

if $r_d = \infty\Omega$

$$Z_o = R_D = 3.3K\Omega$$

with $r_d$

$$A_V = \frac{-g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}} = \frac{-(1.51mS)(3.3K)}{1 + 1.51m \times 1K + \frac{3.3K + 1K}{50K}}$$

$$A_V = -\frac{4.983}{1 + 1.51 + 0.086} = \frac{-4.983}{2.596}$$

$$\boxed{A_V = -1.92}$$

With out $r_d$

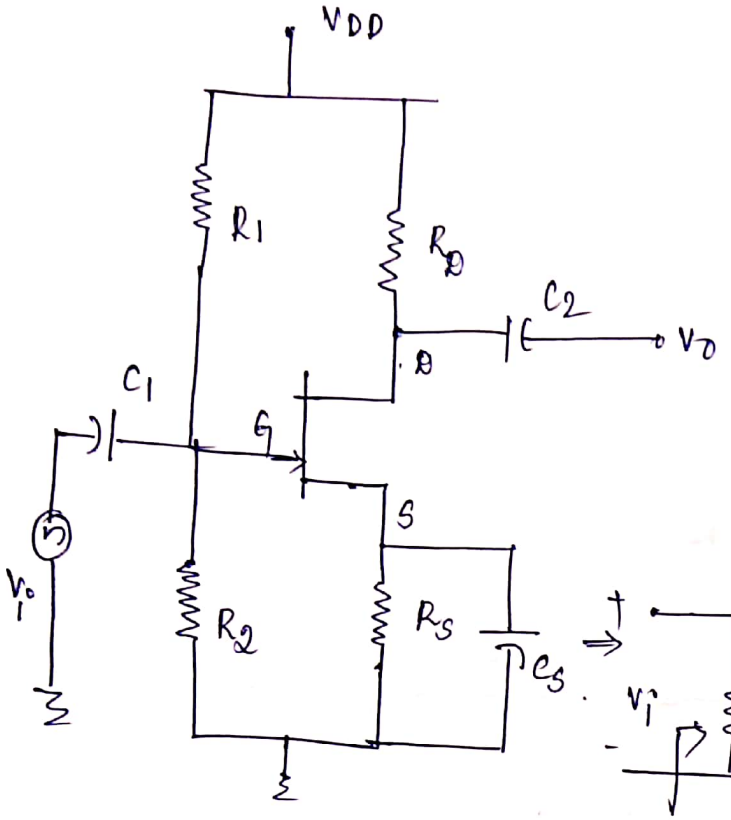
$$A_V = \frac{-g_m R_D}{1 + g_m R_S}$$

$$A_V = \frac{-(1.5\,\text{ms})(3.3\,\text{K})}{1 + 1.5\,\text{ms} \times 1\,\text{K}\Omega}$$

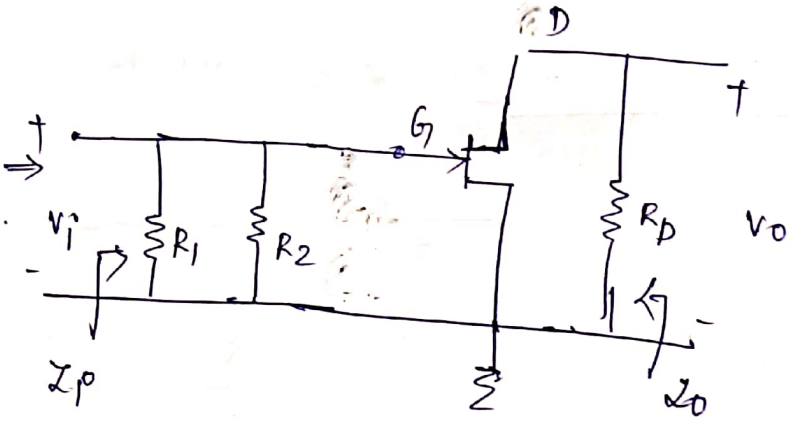
$$\boxed{A_V = -1.98}$$

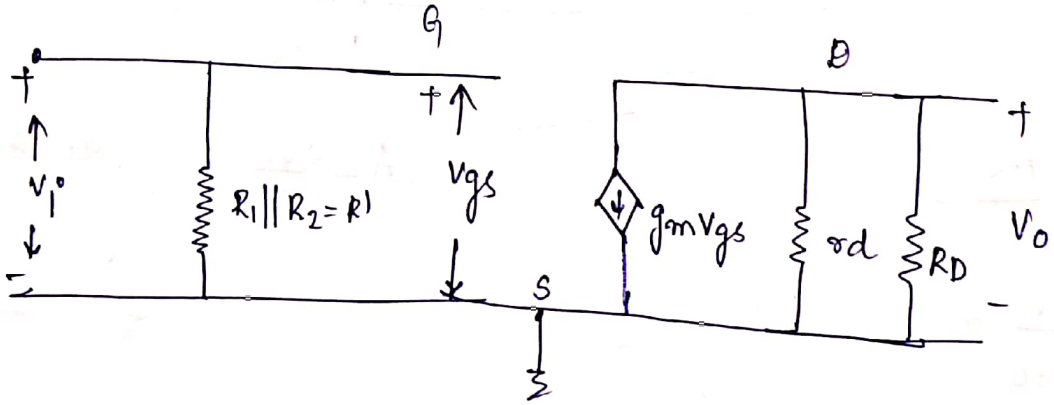
# JFET Voltage Divider Bias






For Ac equivalent ki cuit reduce $V_{DD}$ to Zero & Short ki cuit the Coupling capacitos $C_1$, $C_2$ & $C_S$. As a result $R_1$ & $R_2$ will come in parallel b/w gate and Source.




Ac equivalent ki cuit using small signal ac model of JFET

$Z_i = R' = R_1 \| R_2$

$Z_o$ @ $V_i = 0$, $g_m V_{gs} = 0$ mA,

$$Z_o = r_d \| R_D$$

$$A_V = \frac{V_o}{V_i}$$

$$V_o = -I_o R_L$$

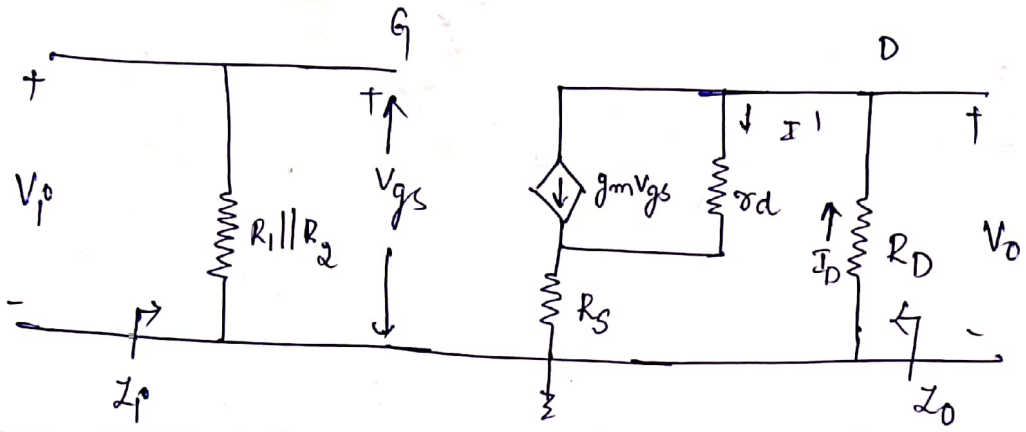
$$V_o = -g_m V_{gs} (r_d \| R_D)$$

$$V_o = -g_m V_i^o (r_d \| R_D)$$

$$\frac{V_o}{V_i^o} = -g_m (r_d \| R_D)$$

$$\boxed{A_V = -g_m (r_d \| R_D)}$$

With unbypassed $R_S$ :




$$\boxed{Z_i^o = R_1 \| R_2}$$

$$A_V = \frac{V_o}{V_i^o} = \frac{-g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

$$Z_o = \frac{V_o}{I_o}$$

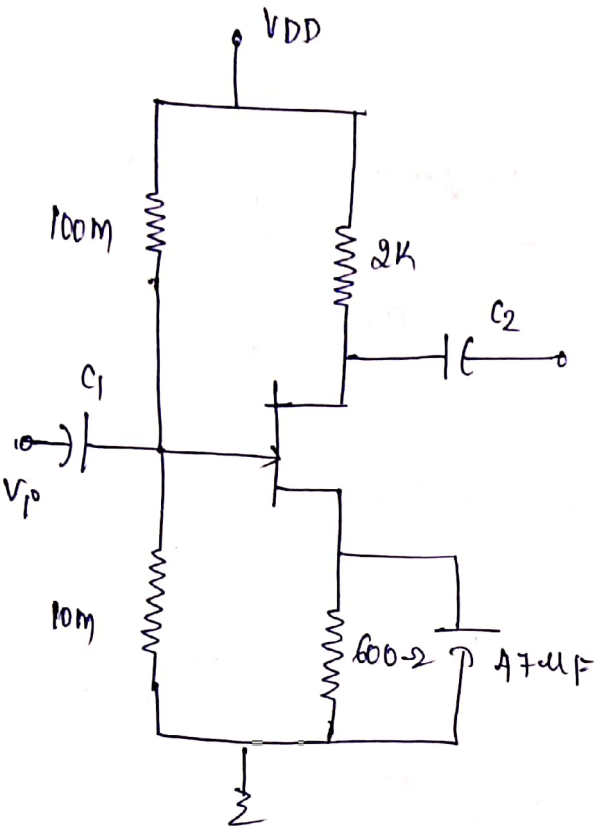
$$Z_o = \frac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}$$

Neglecting the effect of $r_d$

$$\boxed{Z_o = R_D}$$

**Problem**

For JFET Voltage divider bias calculate $Z_i$, $Z_o$, $A_V$ find $V_o$ if $V_i = 25mV$(rms)




$I_{DSS} = 12mA$

$V_p = -3V$

$y_{os} = 10\mu S$

$V_{GSQ} = -1V$

$$g_m = g_{m0}\left(1 - \frac{V_{GSQ}}{V_p}\right)$$

$$g_{m0} = \frac{2\,I_{DSS}}{|V_p|} = \frac{2 \times 12mA}{3}$$

$$\boxed{g_{m0} = 8mS}$$

$$g_m = 8mS\left(1 - \frac{+1}{+3}\right)$$

$$g_m = 8mS\left(1 - \frac{1}{3}\right)$$

$$\boxed{g_m = 5.33mS}$$

$$r_d = 1/y_{os} = 1/10\mu S = \underline{100K\Omega}$$

$$Z_i = R_1 \| R_2 = 100M \| 10M$$

$$\boxed{Z_i = 9.09M\Omega}$$

$$Z_o = r_d \| R_D = 100K\Omega \| 2K$$

$$\boxed{Z_o = 1.96K\Omega}$$

$$A_V = -g_m(r_d \| R_D)$$

$$A_V = 5.33mS(100K \| 2K)$$

$$\boxed{A_V = -10.44}$$

$$V_o = A_V V_i$$

$$= (-10.44) \times 25mV$$

$$\boxed{V_o = -0.261V\,(rms)}$$

With $r_d$

$Z_p = R_1 \| R_2 = 9.09\,K\Omega$

$Z_o = 2K\Omega = R_D$ $\Longrightarrow$ $Z_o = \dfrac{\left[1 + g_m R_S + \dfrac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right]}$

$A_V = \dfrac{-g_m R_D}{1 + g_m R_S}$

$= \dfrac{-(5.33\,mS)(2K)}{1 + (5.33\,mS)(600\Omega)}$

$Z_o = \dfrac{\left[1 + 5.33\,mS \times 600\Omega + \dfrac{600\Omega}{100K}\right] 2K}{\left[1 + 5.33\,mS \times 600\Omega + \dfrac{600\Omega}{100K} + \dfrac{2K}{100K}\right]}$

$\boxed{A_V = -2.53}$

$V_o = A_V V_i$

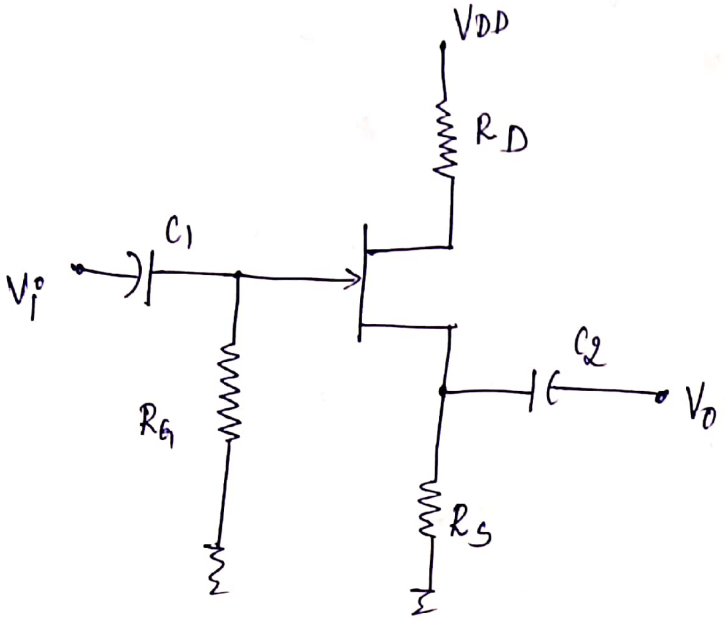
$= -(2.53)(25\,mV)$

$\boxed{V_o = -63.25\,mV\,(rms)}$

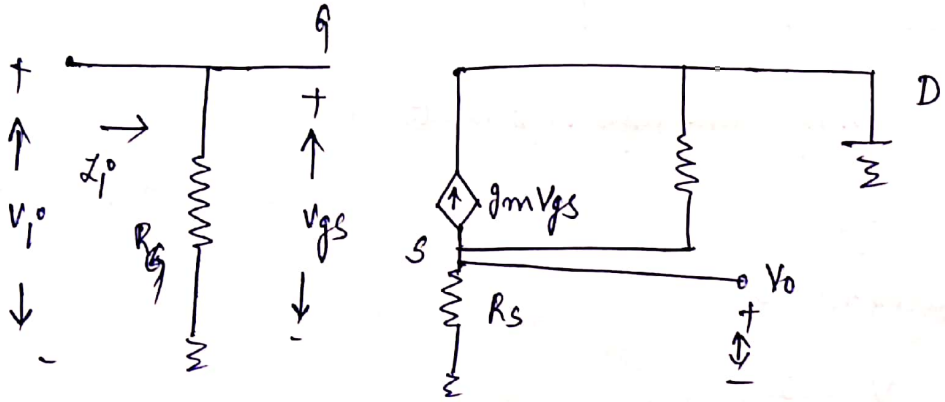
$\boxed{Z_o = 2K\Omega}$

## JFET Source follower (Common drain Configuration)

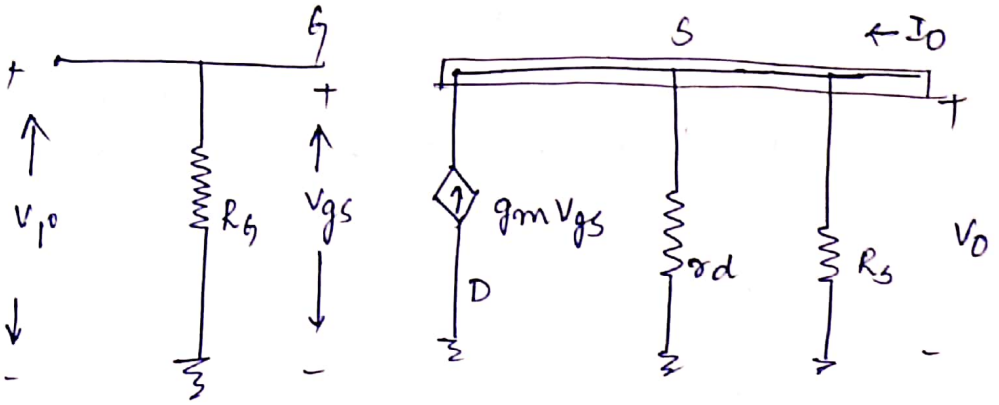
The output is taken off the source terminal & when the dc supply is replaced by its short circuit equivalent the drain is grounded (hence the terminology common drain)




JFET Source follower Configuration

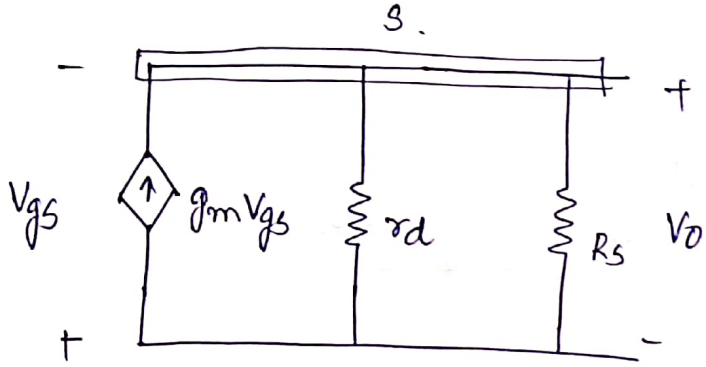



The Controlled Source and the internal output impedance of the JFET are tied to ground at one end and $R_S$ on the other with $V_o$ across $R_S$. Since $g_m V_{gs}$, $r_d$ and $R_S$ are connected to the same terminal and ground they can be placed in parallel. The current source is in reverse direction but $V_{gs}$ is still defined b/w the gate and source terminals.




$$\boxed{I_i = R_G}$$

$I_0$, Setting $V_i = 0$ the resultant ckt is shown below.




$V_{gs}$ & $V_0$ are across the same parallel n/w results in

$$V_0 = -V_{gs}$$

Apply KCL across node S

$$I_0 + g_m V_{gs} = I_{rd} + I_{RS}$$

$$I_0 + g_m V_{gs} = \frac{V_0}{r_d} + \frac{V_0}{R_S}$$

$$I_0 = V_0 \left[ \frac{1}{r_d} + \frac{1}{R_S} \right] - g_m V_{gs}$$

$$I_0 = V_0 \left[ \frac{1}{r_d} + \frac{1}{R_S} \right] - g_m (-V_0)$$

$$\boxed{I_0 = V_0 \left[ \frac{1}{r_d} + \frac{1}{R_S} + g_m \right]}$$

$$Z_o = \frac{V_o}{I_o} = \frac{V_o}{V_o(1/r_d + 1/R_s + g_m)}$$

$$= \frac{1}{1/r_d + 1/R_s + 1/1/g_m}$$

$$\boxed{Z_o = r_d + R_s + 1/g_m}$$ //...

$A_V$ : The output voltage $V_o$ is determined by

$$V_o = I_o R_L$$

$$\boxed{V_o = g_m V_{gs} (r_d \| R_s)} \rightarrow (1)$$

Apply Kirchoffs voltage law around the perimeter of the n/w

$$V_i^o = V_{gs} + V_o$$

$$\boxed{V_{gs} = V_i^o - V_o} \rightarrow (2)$$

Substitute (2) in (1)

$$V_o = g_m (V_i^o - V_o)(r_d \| R_s)$$

$$V_o = (g_m V_i^o - g_m V_o)(r_d \| R_s)$$

$$V_o = g_m V_i^o (r_d \| R_s) - g_m V_o (r_d \| R_s)$$

$$V_o + g_m V_o (r_d \| R_s) = g_m V_i^o (r_d \| R_s)$$

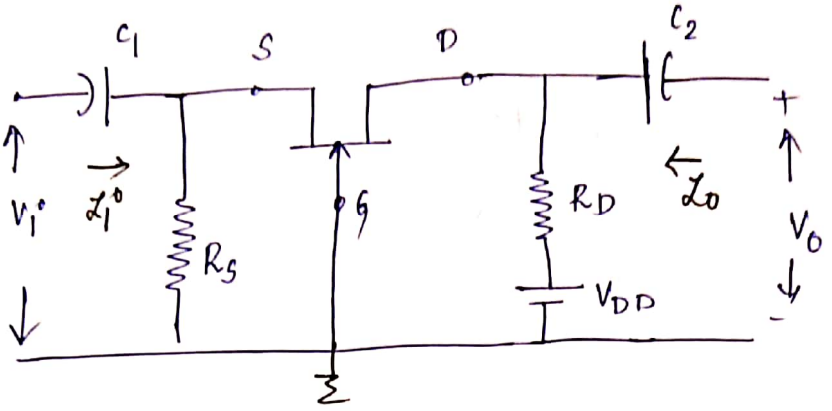
$$V_o (1 + g_m (r_d \| R_s)) = g_m V_i^o (r_d \| R_s)$$

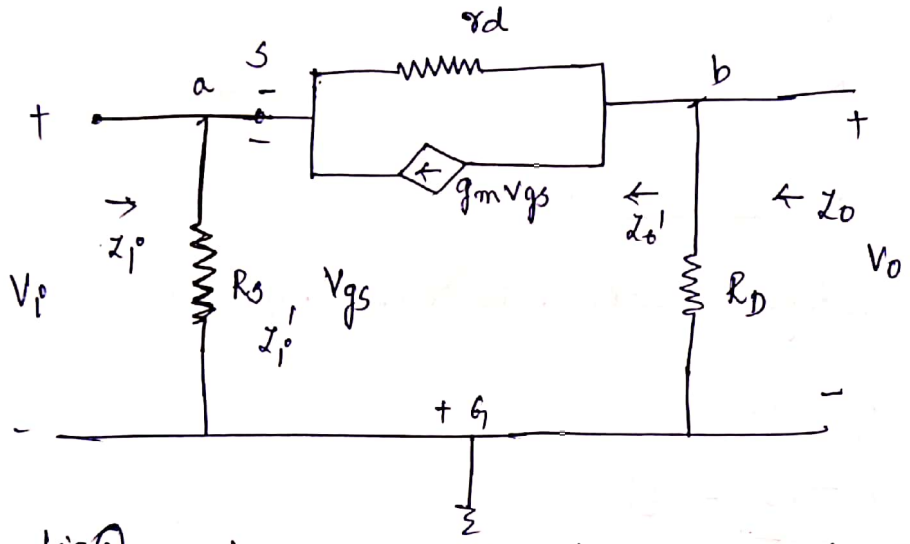
$$\boxed{A_V = \frac{V_o}{V_i^o} = \frac{g_m (r_d \| R_s)}{1 + g_m (r_d \| R_s)}}$$

Positive Sign for $A_V$ reveals that $V_o$ & $V_i$ are in phase.

## JFET Common gate Configuration (10 Marks)

Consider the circuit as shown below.




fig(a) Ac equivalent circuit using JFET Small signal Model.

Controlled Current Source $g_m V_{gs}$ be connected from drain to source with $r_d$ in parallel. The isolation b/w i/p and o/p circuit has been lost since the gate terminal is common ground of the networks

Input impedance : $Z_i' = R_S \| Z_i'^{1}$

where $Z_i'^{1}$ is the impedance looking into source and gate terminals excluding $R_S$.

To find $Z_i'^{1}$ the n/w is redrawn as shown below.

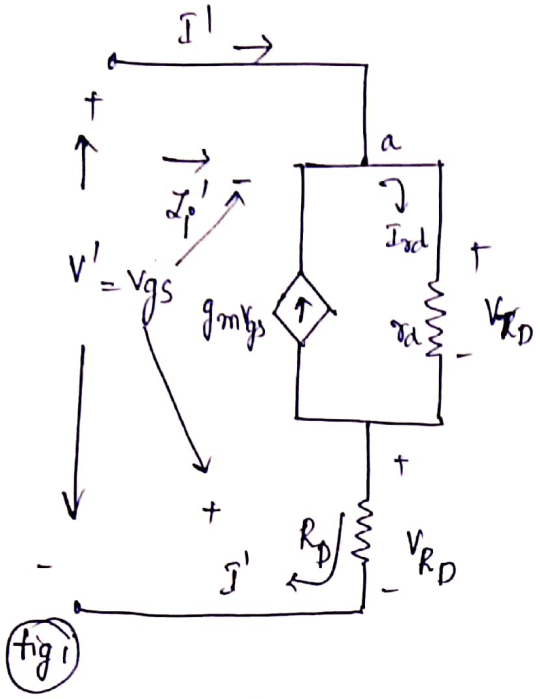



fig 1

The voltage $V' = -V_{gs}$ Apply KVL around the perimeter of the n/w results in

$$V' - V_{rd} - V_{R_D} = 0$$

$$V_{rd} = V' - V_{R_D}$$

$$\boxed{V_{rd} = V' - I' R_D} \rightarrow (1)$$

Apply KCL across node a

$$I' + g_m V_{gs} = I_{rd}$$

$$I_{rd} = \frac{(V' - I' R_D)}{r_d}$$

$$I' = I_{rd} - g_m V_{gs}$$

Substituting $I_{rd}$ in the above equation we get.

$$I' = \frac{(V' - I' R_D)}{r_d} - g_m V_{gs}$$

$$I' = \frac{V'}{r_d} - \frac{I' R_D}{r_d} - g_m (-V')$$

$$I' + \frac{I' R_D}{r_d} = \frac{V'}{r_d} + g_m V'$$

$$I' \left[ 1 + \frac{R_D}{r_d} \right] = V' \left[ \frac{1}{r_d} + g_m \right]$$

$$Z_i' = \frac{V'}{I'} = \frac{\frac{r_d + R_D}{r_d}}{\frac{g_m r_d + 1}{r_d}} = \frac{r_d + R_D}{1 + g_m r_d}$$

$$\boxed{Z_i' = R_S \,||\, \frac{r_d + R_D}{1 + g_m r_d}}$$

If $r_d \geq 10 R_D$ permits the following approximation since $\frac{R_D}{r_d} << 1$

& $1/r_d << g_m$

$$Z_i^{\circ 1} = \frac{\left[1 + \frac{R_D}{r_d}\right]}{\left[g_m + \frac{1}{r_d}\right]}$$

$$\boxed{Z_i^{\circ 1} = 1/g_m}$$

$$\boxed{\therefore Z_i^{\circ} = R_S \,||\, 1/g_m}$$

Output impedance : Substituting $V_i^{\circ} = 0V$ in the figure ① the effects of $R_S$ is shorted out and Set $V_{gs} = 0V$ $\therefore g_m V_{gs} = 0$ $r_d$ will be in parallel with $R_D$.

$$\therefore \boxed{Z_o = r_d \,||\, R_D} \quad r_d \geq 10 R_D$$

$$\boxed{Z_o = R_D}$$

Gain : $A_V = \frac{V_o}{V_i^{\circ}}$ $\boxed{V_i^{\circ} = -V_{gs}}$ from figure ⓐ & $V_o = I_D R_D$

Voltage across $r_d$ is $V_{rd} = V_o - V_i^{\circ}$

$$I_{rd} = \frac{V_o - V_i^{\circ}}{r_d}$$

Apply KCL across node ⓑ in the fig ⓐ we get

$$I_{rd} + I_D + g_m V_{gs} = 0$$

$$I_D = -I_{rd} - g_m V_{gs}$$

$$= -\left[\frac{V_o - V_i^{\circ}}{r_d}\right] - g_m (-V_i^{\circ})$$

$$I_D = \frac{V_i^\circ - V_o}{r_d} + g_m V_i^\circ$$

$$V_o = I_D R_D = \left[ \frac{V_i^\circ - V_o}{r_d} + g_m V_i^\circ \right] R_D$$

$$= \frac{V_i^\circ R_D}{r_d} - \frac{V_o R_D}{r_d} + g_m V_i^\circ R_D$$

$$V_o = \frac{V_i^\circ R_D}{r_d} - \frac{V_o R_D}{r_d} + g_m V_i^\circ R_D$$

$$V_o + \frac{V_o R_D}{r_d} = \frac{V_i^\circ R_D}{r_d} + g_m V_i^\circ R_D$$

$$V_o \left[ 1 + \frac{R_D}{r_d} \right] = V_i^\circ \left[ \frac{R_D}{r_d} + g_m R_D \right]$$

$$A_V = \frac{V_o}{V_i^\circ} = \frac{g_m R_D + \frac{R_D}{r_d}}{\left[ 1 + \frac{R_D}{r_d} \right]}$$

For $r_d \geq 10 R_D$, the factor $R_D/r_d$ can be neglected as a good approximation $\Rightarrow$

$$A_V = g_m R_D \qquad r_d \geq 10 R_D$$

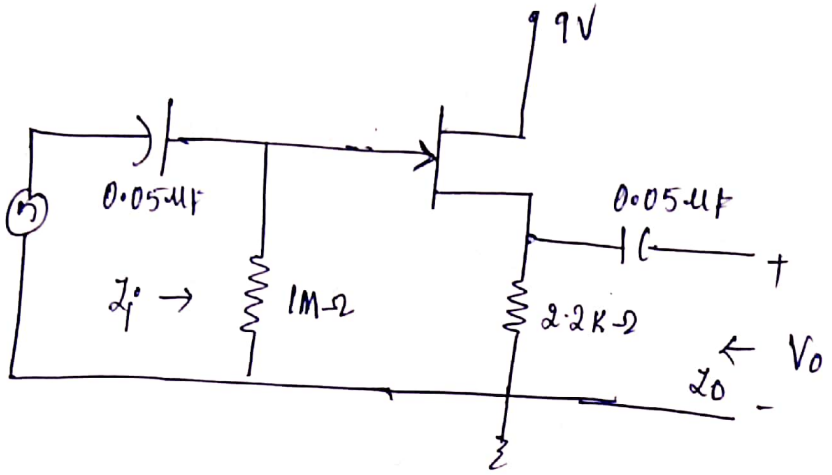
$\therefore$

phase relationship: $A_V$ is +ve will result in an inphase relationship b/w $V_o$ & $V_i^\circ$ for common gate configuration.

## Problem on Common Source Amplifier

1. For a source follower network results in $V_{GSQ} = -2.86\,V$ & $I_{DQ} = 4.56m$

Determine $g_m$, $r_d$, $Z_i$ & also calculate $Z_o$ with & without $r_d$, $A_V$ with and without $r_d$.




$I_{DSS} = 16mA$

$V_p = -4V$

$Y_{os} = 25\mu S$.

$$g_{m0} = \frac{2 I_{DSS}}{|V_p|} = \frac{2 \times 16mA}{4} = 8mS$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_p}\right)$$

$$= 8m\left(1 - \frac{+2.86}{-4}\right)$$

$$\boxed{g_m = 2.28mS}$$

$$r_d = \frac{1}{Y_{os}} = \frac{1}{25\mu S} = 40K\Omega$$

$$Z_i = R_G = 1M\Omega$$

With $r_d$ $\quad Z_o = r_d \,||\, R_S \,||\, 1/g_m$

$$Z_o = 40K \,||\, 2.2K \,||\, 1/2.28mS$$

$$\boxed{Z_o = 362.52\Omega}$$

without rd

$$Z_o = R_S \| 1/g_m$$

$$Z_o = 2.2K \| 1/2.28ms$$

$$\boxed{Z_o = 365.69\Omega}$$

Gain $A_V$

with rd $\quad A_V = \dfrac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$

$$A_V = \frac{2.28m(40K \| 2.2K)}{1 + 2.28m(40K \| 2.2K)}$$

$$A_V = \frac{2.28m(2.09K)}{1 + 2.28m(2.09K)}$$

$$A_V = \frac{4.77}{1+4.77} = 0.83$$

without rd : $\quad A_V = \dfrac{g_m R_S}{1 + g_m R_S}$

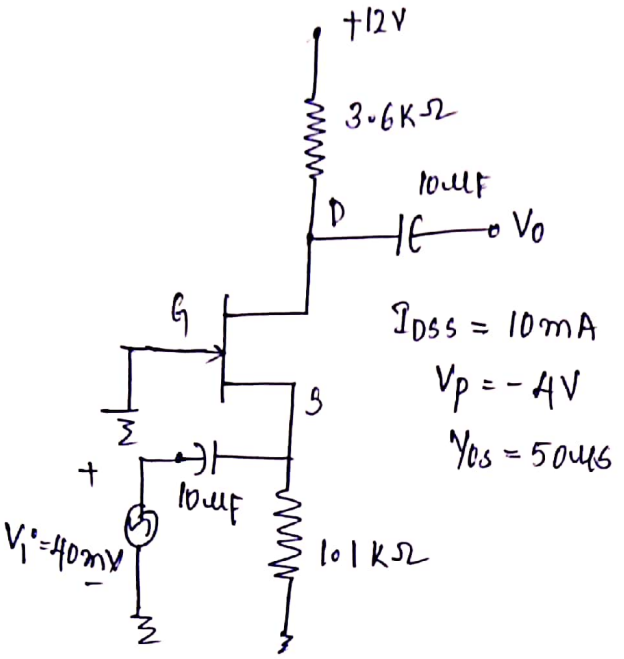
$$A_V = \frac{2.28ms \times 2.2K\Omega}{1 + (2.28ms)(2.2k)}$$

$$A_V = \frac{5.02}{1+5.02}$$

$$\boxed{A_V = 0.83}$$

## Problem on Common gate Configuration

For the figure shown below is a common gate configuration with $V_{GSQ} = -2.2V$ and $I_{DQ} = 2.03mA$, Determine $g_m$, $r_d$. Calculate $Z_i'$ with & without $r_d$ & $Z_o$ determine $V_o$ with and without $r_d$.




$I_{DSS} = 10mA$

$V_p = -4V$

$Y_{os} = 50\mu s$

$$g_{m0} = \frac{2I_{DSS}}{|V_p|}$$

$$g_{m0} = \frac{2 \times 10mA}{4V} = 5ms$$

$$\boxed{g_{m0} = 5ms}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_p}\right)$$

$$= 5ms\left(1 - \frac{+2.2V}{+4}\right)$$

$$= 5ms\left(1 - \frac{2.2}{4}\right)$$

$$\boxed{g_m = 2.25ms}$$

$$r_d = \frac{1}{Y_{os}} = \frac{1}{50\mu s} = 20K\Omega$$

① with $r_d$

$$Z_i' = R_S \,||\, \left[\frac{r_d + R_D}{1 + g_m r_d}\right]$$

$$= 1.1K \,||\, \left[\frac{20K + 3.6K\Omega}{1 + 2.25m\,(20K)}\right]$$

$$= 1.1K \,||\, 0.51K$$

$$\boxed{Z_i' = 0.35K\Omega}$$

without $r_d$:

$$Z_i' = R_S \,||\, 1/g_m = 1.1K \,||\, 1/2.25ms = 1.1K\Omega \,||\, 0.44K\Omega$$

$$\boxed{Z_i' = 0.31K\Omega}$$

With rd $Z_0 = R_D \| r_d$

$Z_0 = 3.6K \| 20K\Omega$

$\boxed{Z_0 = 3.05K\Omega}$

Without rd

$\boxed{Z_0 = R_D = 3.6K\Omega}$

$A_V$ : Gain : with rd

$$A_V = \frac{g_m R_D + \frac{R_D}{r_d}}{\left[1 + \frac{R_D}{r_d}\right]}$$

$$A_V = \frac{(2.25m)(3.6K) + (3.6K/20K)}{1 + \left(\frac{3.6K}{20K}\right)}$$

$$A_V = \frac{8.1 + 0.18}{1 + 0.18} = 7.02$$

$$A_V = \frac{V_o}{V_i}$$

$V_o = A_V V_i = 7.02 \times 40mV = 280.8mV$

without rd :

$A_V = g_m R_D = 2.25m \times 3.6K = 8.1$

$V_o = A_V V_i = (8.1) \times 40mV$

$\boxed{V_o = 324mV}$

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## Module 4: Feedback and oscillator Circuits.

Feedback: feedback is a process of Supplying a part of the output back to the input. In transistor amplifier a fraction of the output voltage may feedback to the input terminals.

Two types of feedback:

1. Positive feedback:
2. Negative feedback.

Positive feedback: Both input and output are in same phase.

Negative feedback: Both input and output are in out phase.

positive feedback increases the gain of an amplifier but it increases distortion and gain instability.

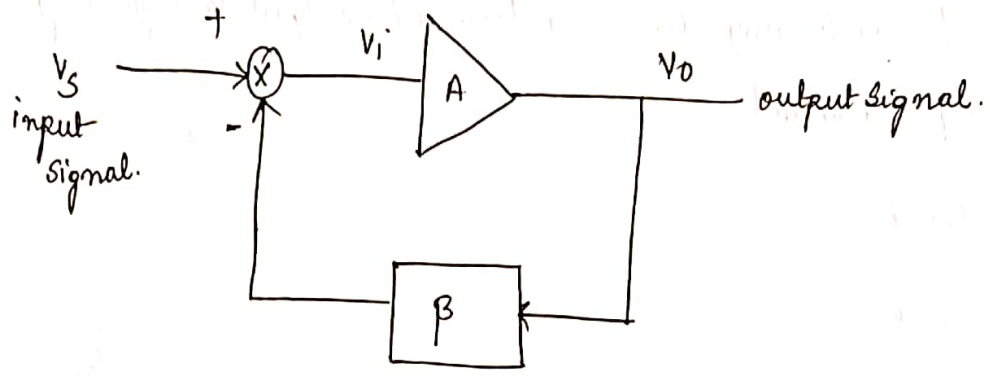
Negative feedback decreases the gain but it reduces distortion and noise lend

The negative feedback have following advantages

1. Higher input Impedance
2. Better stabilized voltage gain
3. Improved frequency response.
4. Lower output Impedance
5. Reduced noise and More linear operation.

The feedback Connection is as shown below the input signal $V_s$ is applied to a Mixer network where it is combined with a feedback signal $V_f$. The difference of these signals $V_i$ is the input voltage to the amplifier.

A portion of the amplifier output $V_o$ is connected to the feedback network ($\beta$) which provides a reduced portion of the output as feedback signal to the input mixer network




Block diagram of feedback amplifier.

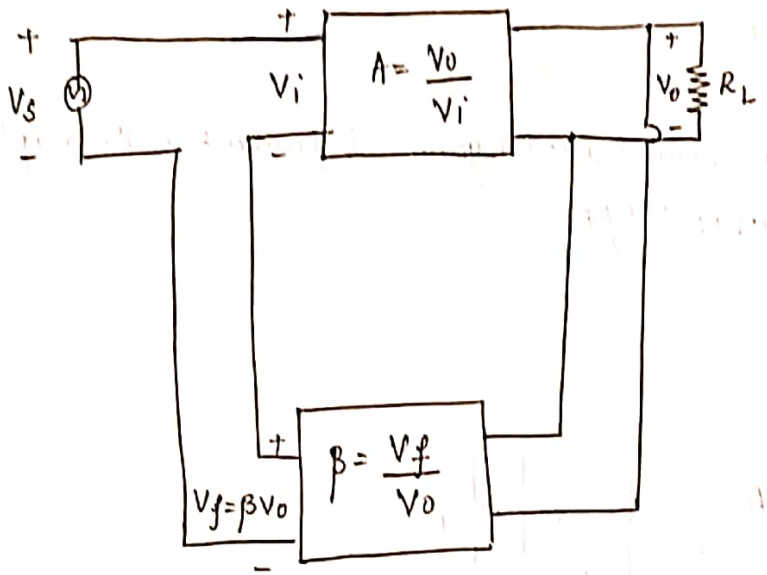
Feedback Connection types: There are four basic ways of Connecting the feedback signal. Both voltage and current can be feedback to the input either in series or parallel.

① Voltage Series feedback
② Voltage Shunt feedback
③ Current Series feedback
④ Current Shunt feedback.

Voltage refers to Connecting the output voltage as input to the feedback network. Current refers to tapping off some output current through the feedback network. Series refers to connecting the feedback signal in series with the input signal voltage. Shunt refers to connecting the feedback signal in shunt (parallel) with an input current source.

Series feedback Connections are used to increase the input resistance and Shunt feedback connection are used to decrease the input resistance.

Voltage feedback decreases the output impedance where as Current increases the output impedance




Voltage Series feedback gain with feedback : Figure above shows the voltage series feedback connection with a part of the output voltage fed back in series with the input signal resulting in an overall gain reduction. If there is no feedback ($V_f = 0$) the voltage gain of the amplifier stage is

$$A = \frac{V_o}{V_S} = \frac{V_o}{V_i} \quad \rightarrow (1)$$

If a feedback signal $V_f$ is connected in series with input then

$$V_i = V_S - V_f$$

From equation (1)

$$V_o = AV_i$$

$$= A(V_S - V_f)$$

$V_f = \beta V_o$ from feedback network

$$V_o = AV_S - AV_f$$

$$V_o = AV_S - A\beta V_o$$

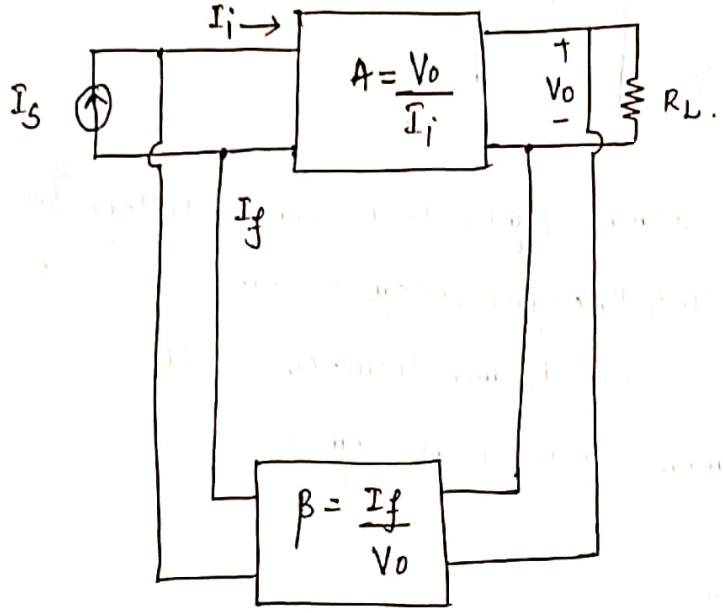
$$V_o + A\beta V_o = AV_S$$

$$V_o(1 + A\beta) = AV_S$$

$$A_f = \frac{V_o}{V_s} = \frac{A}{1+A\beta}$$

The above equation shows that the gain with feedback is the amplifier gain reduced by the factor of $(1+\beta A)$.

## Voltage Shunt feedback:




The gain of the feedback for the network is

$$A_f = \frac{V_o}{I_s}$$

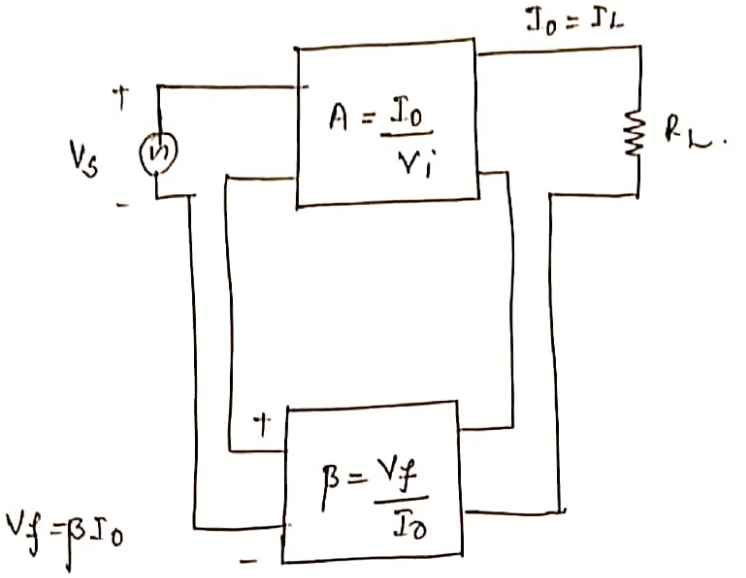
$$A_f = \frac{A I_i}{I_i + I_f}$$

$$A_f = \frac{A I_i}{I_i + \beta V_o}$$

$$A_f = \frac{A I_i}{I_i + \beta A I_i} = \frac{A I_i}{I_i (1+\beta A)}$$

$$\boxed{A_f = \frac{A}{1+\beta A}} \quad //..$$

## Current Series feedback :



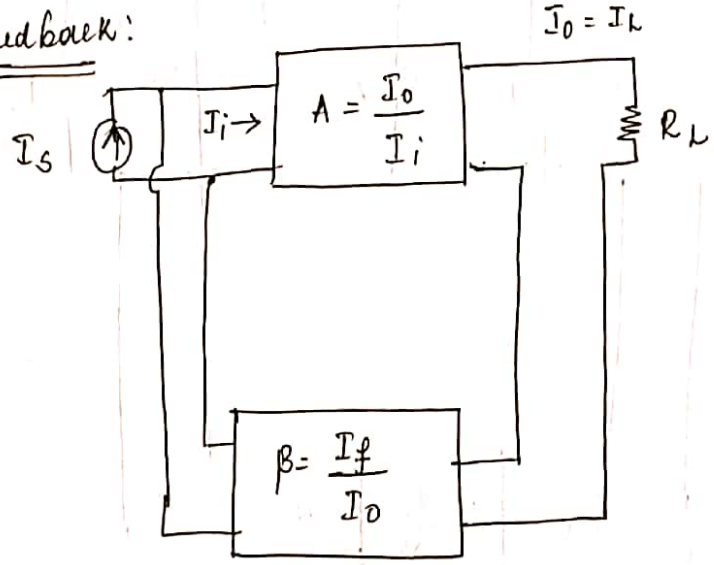

$$A_f = \frac{I_0}{V_s}$$

$$A_f = \frac{I_0}{V_i + V_f}$$

$$A_f = \frac{I_0}{V_i + \beta I_0} = \frac{A V_i}{V_i + \beta A V_i} = \frac{A V_i}{V_i (1 + A\beta)} = \frac{A}{1 + A\beta}$$

$$\boxed{A_f = \frac{A}{1 + A\beta}}$$

## Current Shunt feedback :



$$A_f = \frac{I_o}{I_s}$$

$$A_f = \frac{I_o}{I_i + I_f}$$

$$A_f = \frac{I_o}{I_i + \beta I_o}$$

$$A_f = \frac{I_o}{I_i + \beta A I_i}$$

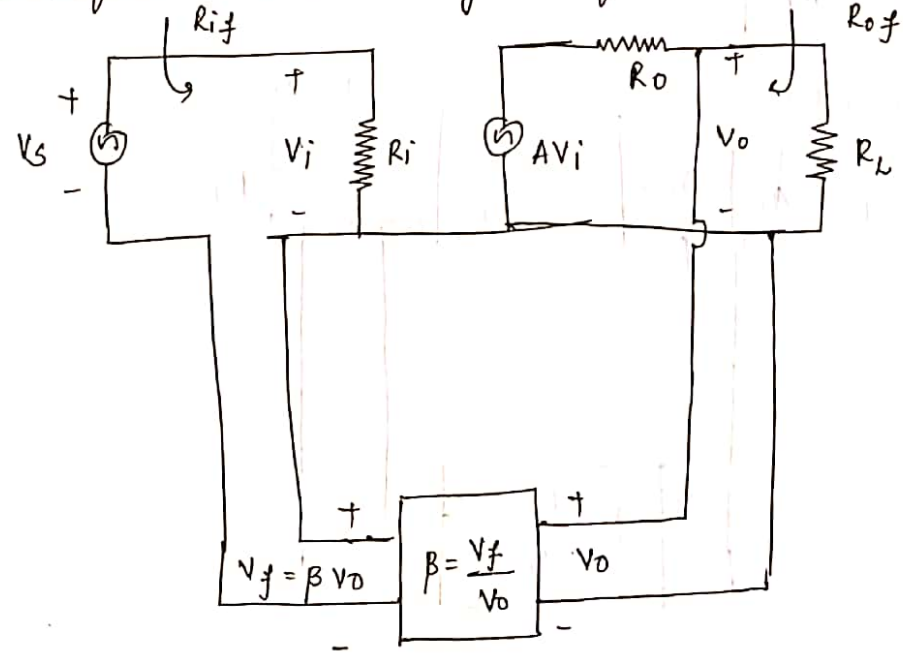
$$A_f = \frac{A I_i}{I_i (1 + A\beta)} = \frac{A}{1 + A\beta}$$

$$\boxed{A_f = \frac{A}{1 + A\beta}}$$

∴

## Input Impedance and output Impedance with feedback

Voltage Series feedback: Consider voltage-Series feedback Connection.



The input impedance can be determined as follows.

$$I_i = \frac{V_i}{Z_i} = \frac{V_s - V_f}{I_i}$$

$$I_i = \frac{V_s - \beta V_o}{I_i} = \frac{V_s - \beta A V_i}{I_i}$$

$$Z_i I_i = V_s - \beta V_o = V_s - \beta A V_i$$

$$Z_i I_i = V_s - \beta A V_i$$

$$Z_i I_i = V_s - \beta A Z_i I_i$$

$$Z_i I_i (1 + \beta A) = V_s$$

$$\boxed{Z_{if} = \frac{V_s}{I_i} = Z_i (1 + \beta A)}$$

$$\boxed{Z_{if} = Z_i (1 + A\beta)}$$

$\because$

$\because$ KVL

$$I_i = \frac{V_i}{Z_i}$$

$$V_i = I_i Z_i$$

$Z_i$ = Input-Impedance without feedback

$Z_{if}$ = I/p Impedance with feedback

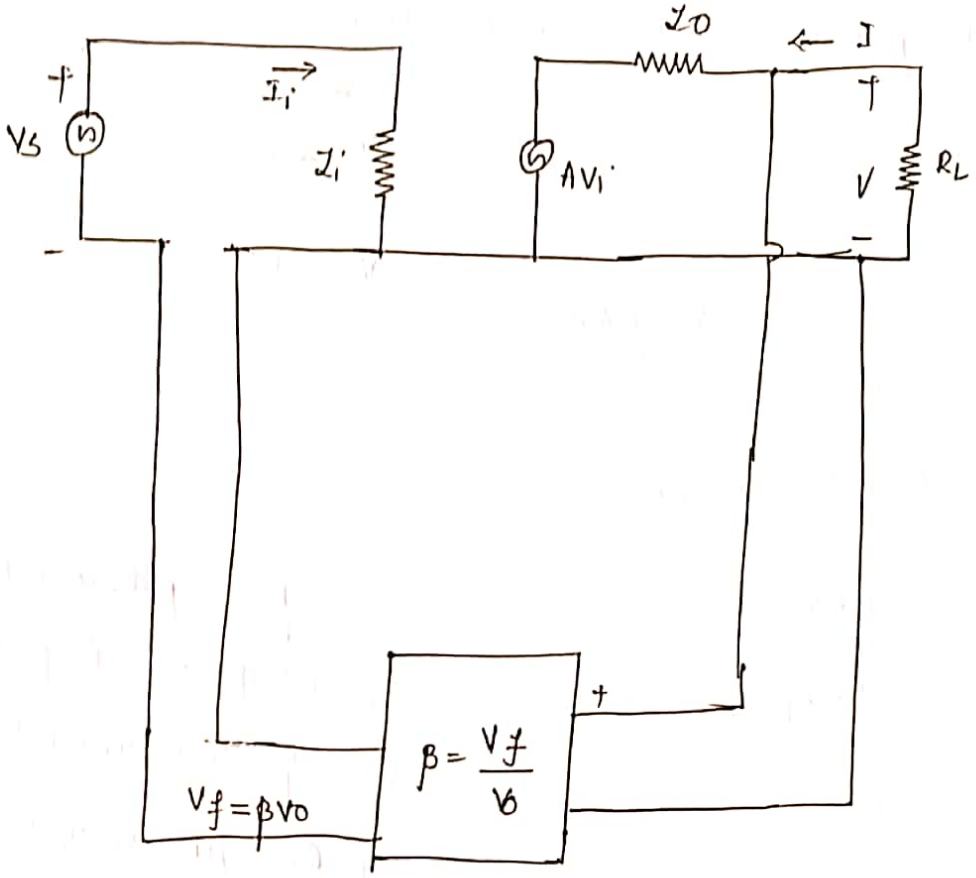
$Z_o$ = output Impedance without feedback

$Z_{of}$ = O/p Impedance with feedback.

The input Impedance with Series feedback is seen to be the value of the input Impedance without feedback multiplied by the factor $(1+\beta A)$ and applies for both Voltage and current Series.

Output Impedance with feedback :-

For Voltage feedback the output impedance is decreased the output impedance is determined by applying a voltage V resulting in a Current I with $V_s$ is Shorted out.




$$V = I Z_o + A V_i$$

$$V = I Z_o + A(-V_f)$$

$$V = I Z_o - A V_f$$

$$V = I Z_o - A\beta V$$

$$V + A\beta V = I Z_o$$

$$V(1 + A\beta) = I Z_o$$

$$Z_{of} = \frac{V}{I} = \frac{Z_o}{1 + A\beta}$$

$$\boxed{Z_{of} = \frac{Z_o}{1 + A\beta}}$$

For $V_s = 0$

$$V_i = V_s - V_f$$

$$V_i = 0 - V_f$$

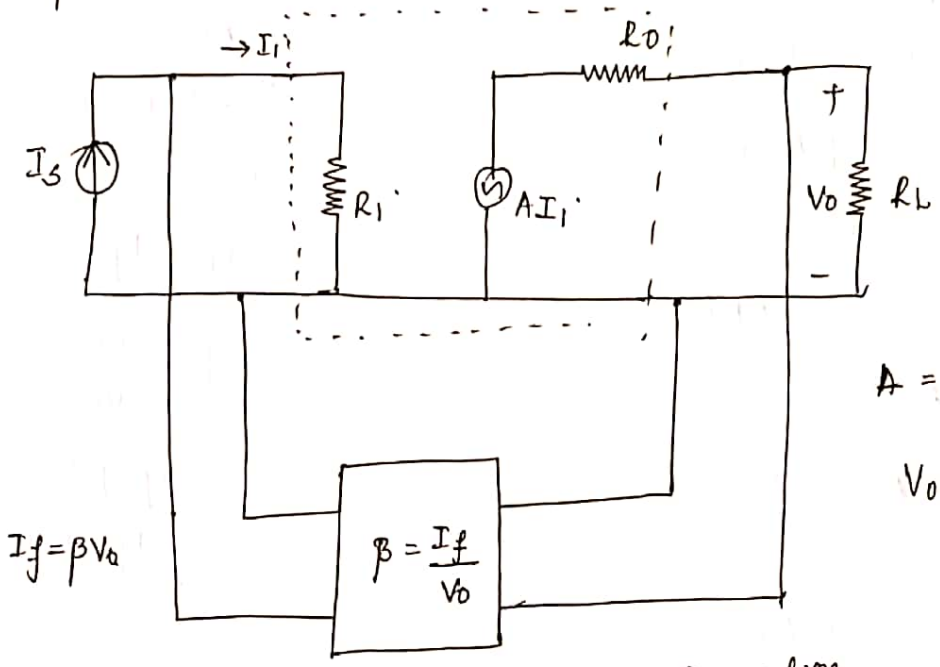
$$V_i = -V_f$$

$$V_f = \beta V_o \quad , V_o = V$$

$$\boxed{V_f = \beta V}$$

Voltage shunt feedback : Input Impedance and output Impedance

The i/p Impedance can be determined to be.




$A = \frac{V_o}{V_i}$

$V_o = A I_i$

Voltage shunt feedback connection.

Input Impedance with feedback $Z_{if} = \frac{V_i}{I_S}$

$$I_S = I_i + I_f$$

$$Z_{if} = \frac{V_i}{I_i + I_f} = \frac{V_i}{I_i + \beta V_o}$$

Divide Numerator and denominator by $I_i$

$$Z_{if} = \frac{V_i / I_i}{I_i / I_i + \beta V_o / I_i}$$

$Z_i = \frac{V_i}{I_i}$

$$\boxed{Z_{if} = \frac{Z_i}{1 + A\beta}}$$

The voltage shunt feedback amplifier the input impedance gets reduced by the factor $(1 + A\beta)$

Output Impedance : The o/p Impedance is determined by applying V resulting in a current I with $V_s = 0$ & $I_s = 0$

$$V = I Z_0 + A I_i$$

$$V = I Z_0 + A I_i$$

$$V = I Z_0 - A I_f$$

$$V = I Z_0 - A\beta V$$

$$V + A\beta V = I Z_0$$

$$V(1 + A\beta) = I Z_0$$

$$\frac{V}{I} = \frac{Z_0}{1 + A\beta}$$

$$Z_{of} = \frac{V}{I} = \frac{Z_0}{1 + A\beta}$$

WKT

$$I_s = I_i + I_f$$

$$I_s = 0$$

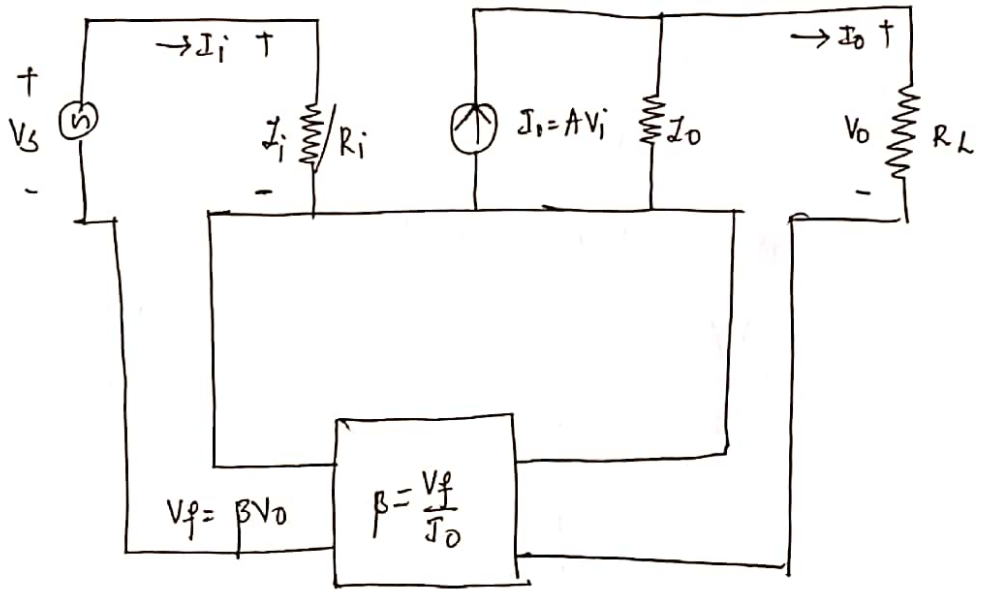
$$I_i = -I_f$$

$$\beta = \frac{I_f}{V_0}$$

$$I_f = \beta V_0$$

$$I_f = \beta V$$

Input Impedance of Current Series feedback




$$Z_i = \frac{V_i}{I_i}$$

$$Z_i = \frac{V_s - V_f}{I_i}$$

$$V_i = V_s - V_f$$

$$\beta = V_f / I_0$$

$$V_f = \beta I_0$$

$$Z_i = \frac{V_s - V_f}{I_i}$$

$$Z_i I_i = V_s - V_f$$

$$Z_i I_i = V_s - \beta V_o$$

$$Z_i I_i = V_s - \beta A V_i$$

$$Z_i I_i = V_s - \beta A Z_i I_i$$

$$Z_i I_i + \beta A Z_i I_i = V_s$$

$$Z_i I_i (1 + A\beta) = V_s$$

$$Z_{if} = \frac{V_s}{I_i} = Z_i (1 + A\beta)$$

$$\boxed{Z_{if} = Z_i (1 + A\beta)}$$

Replace in o/p ckt

$V_o = V$

$I_o = I$

**Output Impedance :** $V_s = 0$

$V_s = V_i - V_f$

$0 = V_i - V_f$

$V_i = V_f$

Let a voltage V be applied to the output port and I denote the resulting current.

By applying KCL at the o/p loop

$$I = \frac{V}{Z_o} - AV_i$$

$$I = \frac{V}{Z_o} - AV_f$$

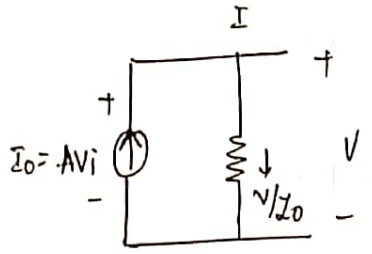
$$I = \frac{V}{Z_o} - A\beta I$$

$$I + A\beta I = \frac{V}{Z_o}$$

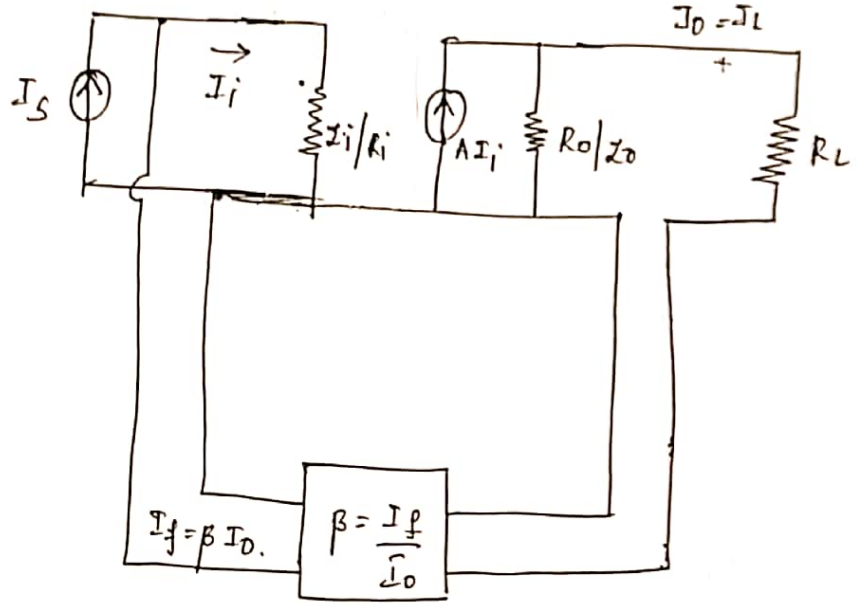
$$I (1 + A\beta) = V/Z_o$$

$$V = I Z_o (1 + A\beta)$$

$$\boxed{Z_{of} = \frac{V}{I} = Z_o (1 + A\beta)}$$



## Current Shunt feed back




Input Impedance and output impedance:

$$Z_{if} = \frac{V_i'}{I_S} = \frac{V_i}{I_i + I_f} = \frac{V_i / I_i}{I_i / I_i + \beta I_f / I_i}$$

$$\boxed{Z_{if} = \frac{Z_i}{1 + A\beta}}$$

Consider the output ---------- : circuit of Current Shunt feed back.

$$I = \frac{V}{Z_o} - AI_i'$$

$$= \frac{V}{Z_o} - AI_f$$

$$I = \frac{V}{Z_o} - A\beta I$$

$$I + A\beta I = \frac{V}{Z_o}$$

$$I(1 + A\beta) = \frac{V}{Z_o}$$

$$\boxed{\frac{V}{I} = Z_o(1 + A\beta)}$$

$$\boxed{Z_{of} = Z_o(1 + A\beta)}$$ //.

$I_S = I_i + I_f$ or

Consider the below equation.

$$I_i' = I_S + I_f$$

$$I_i' = I_f$$

$$\beta = \frac{I_f}{I_o}$$

$$I_f = \beta I$$

→ Determine the voltage gain, input and output impedance with feedback for voltage series feedback having $A = -100$, $R_i = 10K\Omega$, $R_o = 20K\Omega$ for feedback of $\beta = -0.1$ & $\beta = -0.5$.

$\beta = -0.1$

$$A_f = \frac{A}{1+A\beta} = \frac{-100}{1+(-0.1)(-100)} = \frac{-100}{11} = -9.09$$

$$Z_{if} = Z_i(1+\beta A) = 10K\Omega(11) = 110K\Omega$$

$$Z_{of} = \frac{Z_o}{1+A\beta} = \frac{20\times10^3}{1+(100)(-0.1)} = 1.82K\Omega$$

$\beta = -0.5$

$$A_f = \frac{A}{1+A\beta} = \frac{-100}{1+(-0.5)(-100)} = \frac{-100}{51} = -1.96$$

$$Z_{if} = Z_i(1+A\beta) = 10K\Omega(51) = 510K\Omega$$

$$Z_{of} = Z_o/1+A\beta = \frac{20\times10^3}{51} = 392.16\Omega$$

practical feedback circuits : Voltage Series feedback

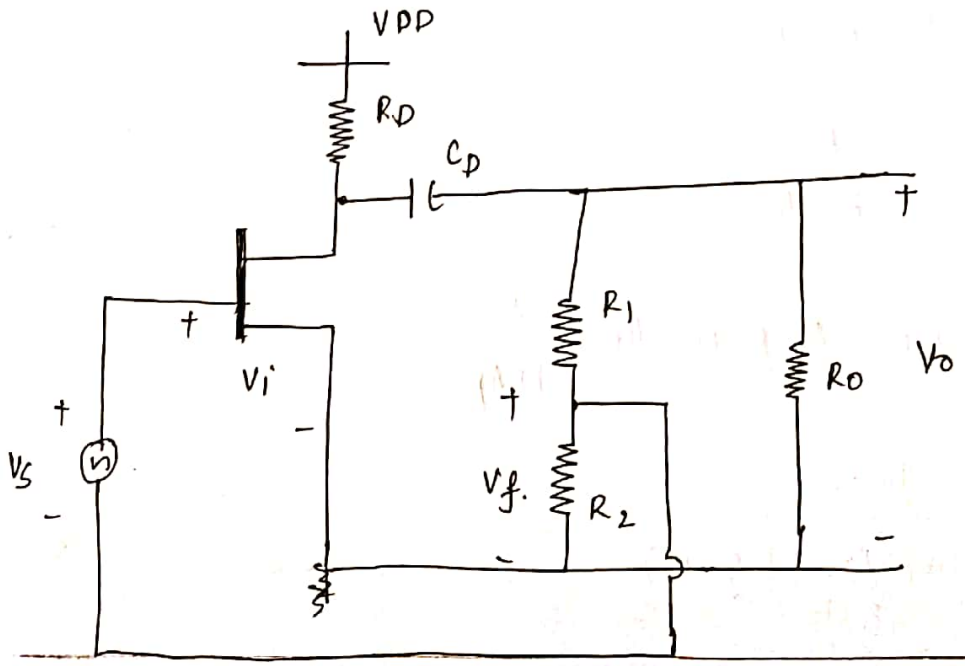


Figure below shows an FET amplifier stage with voltage series feedback. A part of the o/p signal $V_o$ is obtained using a feedback network of resistors $R_1$ and $R_2$

The feedback voltage $V_f$ is connected in series with the source signal $V_s$ their difference being the input signal $V_i$

Without feedback the amplifier gain

$$A = \frac{V_o}{V_i} = -g_m R_L \rightarrow (1)$$

For AC analysis Consider $V_{DD} = 0$

$R_D$ is analysed wrt to ground.

Consider that has load resistance

$$R_L = R_D \, R_0 \, (R_1 + R_2) \rightarrow (2)$$

The feedback network provides a feedback factor of $\beta$

$$\beta \Rightarrow V_o = \frac{-V_f R_2}{R_1 + R_2}$$

$$\frac{V_o}{V_f} = \frac{R_2}{R_1 + R_2}$$

$$\beta = \frac{-R_2}{R_1 + R_2}$$

using the values of A & $\beta$ in $A_f = \frac{A}{1 + A\beta}$

$$A_f = \frac{-g_m R_L}{1 + \left(\frac{-R_2}{R_1 + R_2}\right)(-g_m R_L)}$$

$$A_f = \frac{-g_m R_L}{1 + \frac{g_m R_2 R_L}{R_1 + R_2}} = \frac{-g_m R_L}{\frac{R_1 + R_2 + g_m R_2 R_L}{R_1 + R_2}} = \frac{-g_m R_L (R_1 + R_2)}{R_1 + R_2 + g_m R_2 R_L}$$

$$A_f = \frac{-g_m R_L (R_1 + R_2)}{\left(\frac{(R_1 + R_2)}{g_m R_L} + R_2\right) g_m R_L}$$

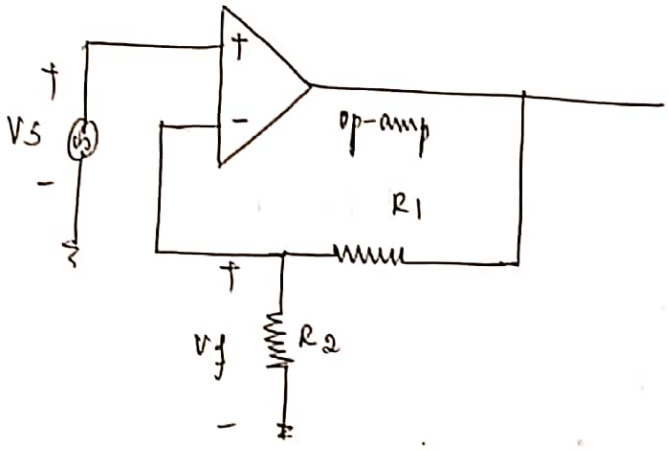
$$A_f = \frac{-(R_1 + R_2)}{\left(\frac{R_1 + R_2}{g_m R_L} + R_2\right)}$$

$R_2 >> \frac{R_1 + R_2}{g_m R_L}$

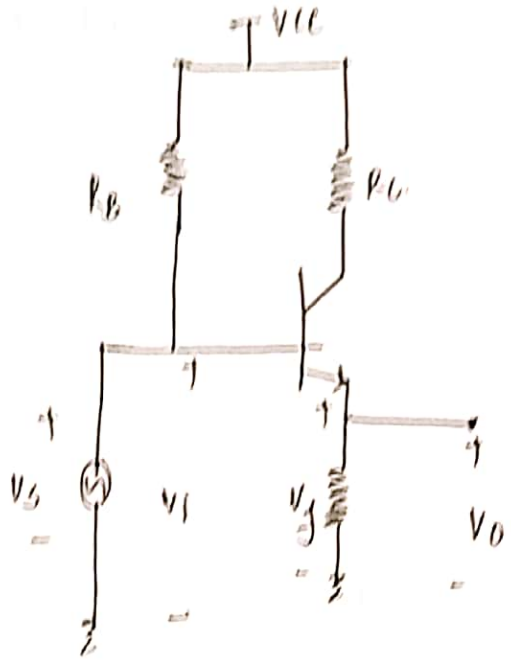
$$\boxed{A_f = \frac{-(R_1 + R_2)}{R_2}}$$

Below figure shows the voltage series feedback connection using op-amp. The gain of the op-amp A without feedback is reduced by the feedback factor

$$\beta = \frac{R_2}{R_1 + R_2}$$



Consider the emitter follower as shown below provides voltage series feedback




The signal voltage $V_s$ is the input voltage $V_i$. The o/p voltage $V_o$ is also the feedback voltage in series with the input voltage. The amplifier shown here provides the operation with feedback. The operation of the circuit without feedback provides $V_f = 0$

$$A = \frac{V_o}{V_s} = \frac{h_{fe} I_b R_E}{V_s}$$

$$= \frac{h_{fe} I_b R_E}{V_s}$$

$$= \frac{h_{fe} \cdot V_s / h_{ie} R_E}{V_s}$$

$$\boxed{A = \frac{h_{fe} R_E}{h_{ie}}}$$

$$\beta = \frac{V_f}{V_o} = 1$$

WKT $A_f = \frac{A}{1 + A\beta} = \frac{h_{fe} R_E / h_{ie}}{1 + h_{fe} R_E / h_{ie}}$

$$= \frac{h_{fe} R_E / h_{ie}}{\frac{h_{ie} + h_{fe} R_E}{h_{ie}}}$$

$$A_f = \frac{h_{fe} R_E}{h_{ie} + h_{fe} R_E} \approx \frac{h_{fe} R_E}{h_{fe} R_E} \approx 1$$

WKT

$I_c \approx I_E$

$I_c = \beta I_b = h_{fe} I_b$

Proved $V_o = I_E R_E$

$$\boxed{V_o = h_{fe} I_b R_E}$$

$I_b = \frac{V_s}{h_{ie}}$

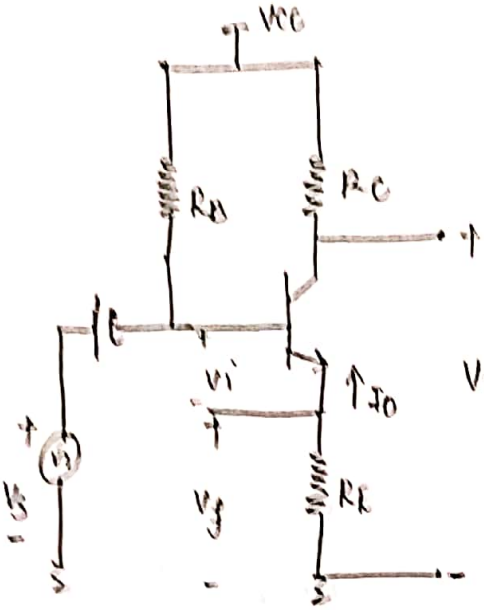
If

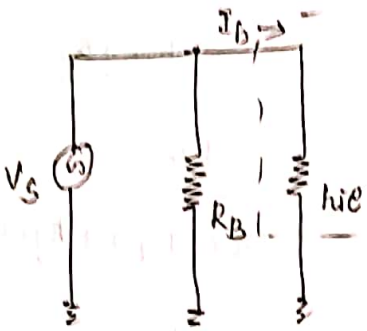
$R_E h_{fe} \gg h_{ie}$

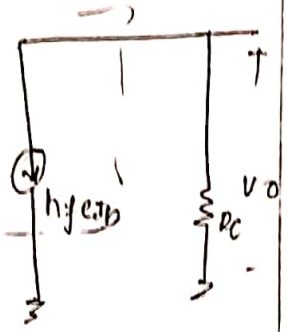
Current series feedback : In this feedback technique the sample output current $I_o$ and returns a proportional voltage in series with the input. The current series feedback connection increases input resistance.

Consider the figure as shown below single stage transistor amplifier, Since the emitter of this stage has an unbypassed emitter it effectively have current series feedback.

The current through resistor $R_E$ results in a feedback voltage that opposes the source signal applied so that o/p $V_o$ is reduced.




WKT $I_o = I_c$

$= \beta \cdot I_b$

$I_o = h_{fe} I_b$

Neglecting the value of $I_b$

Without feedback: WKT $A = \frac{I_o}{V_i} = \frac{-I_b h_{fe}}{I_b h_{ie} + R_E}$

$$A = \frac{-h_{fe}}{h_{ie} + R_E}$$

$$\beta = \frac{V_f}{I_o} = \frac{-I_o R_E}{I_o} = -R_E$$

The input and output impedances are respectively

$$Z_i = R_B \,||\, (h_{ie} + R_E) \simeq h_{ie} + R_E$$

$Z_o = R_c$

With feed back : $A_f = \frac{I_o}{V_s} = \frac{A}{1+A\beta}$

$$A_f = \frac{-h_{fe}/h_{ie}+R_E}{1+(-R_E)\left(\frac{-h_{fe}}{h_{ie}+R_E}\right)}$$

$$= \frac{-h_{fe}/h_{ie}+R_E}{1+h_{fe}R_E/h_{ie}+R_E}$$

$$= \frac{-h_{fe}/h_{ie}+R_E}{(h_{ie}+R_E)+h_{fe}R_E}$$

$$= \frac{-h_{fe}}{(h_{ie}+R_E)+h_{fe}R_E}$$

$$A = \frac{-h_{fe}}{(h_{ie}+R_E)+h_{fe}R_E}$$

If $h_{ie}+R_E \overset{n}{=} h_{ie}$

$$\boxed{A = \frac{-h_{fe}}{h_{ie}+h_{fe}R_E}}$$

The input and output Impedance are calculated as specified below

$$Z_{if} = Z_i(1+\beta A) = h_{ie}\left(1+\frac{h_{fe}R_E}{h_{ie}}\right) = h_{ie}+h_{fe}R_E$$

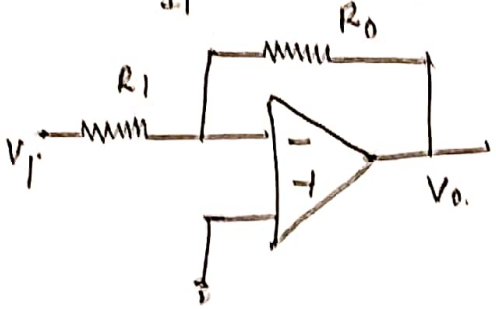
$$Z_{of} = Z_o(1+\beta A) = R_C\left(1+\frac{h_{fe}R_E}{h_{ie}}\right)$$

The voltage gain $A_f$ with feedback.

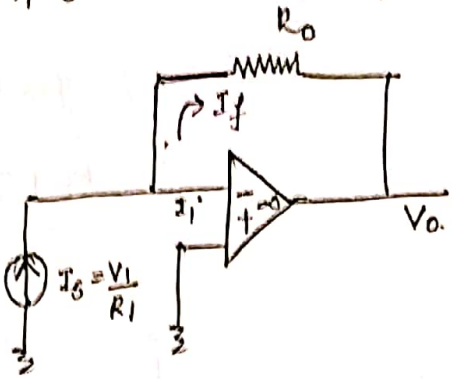
$$A_{vf} = \frac{V_o}{V_s} = \frac{I_o R_c}{V_s} = \frac{I_o}{V_s} R_c = A_f R_c = \frac{-h_{fe} R_c}{h_{ie} + h_{fe} R_E}$$

**Voltage Shunt feedback:** The Constant gain op-amp circuit provides a voltage shunt feedback for an op amp ideal characteristics $I_i = 0$, $V_i = 0$ and voltage gain of infinity

$$A = \frac{V_o}{I_i} = \infty \quad , \beta = \frac{I_f}{V_o} = \frac{-1}{R_0}$$




Constant gain circuit




Equivalent circuit.

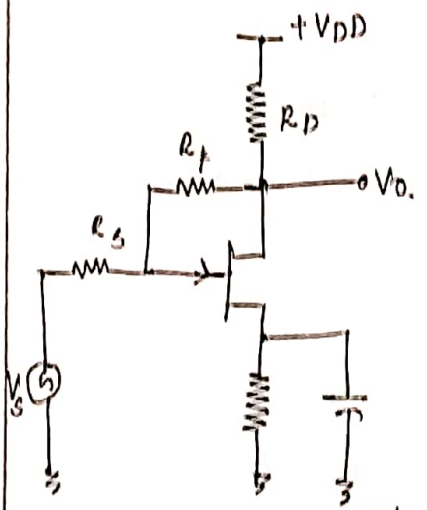
The gain with feedback is then

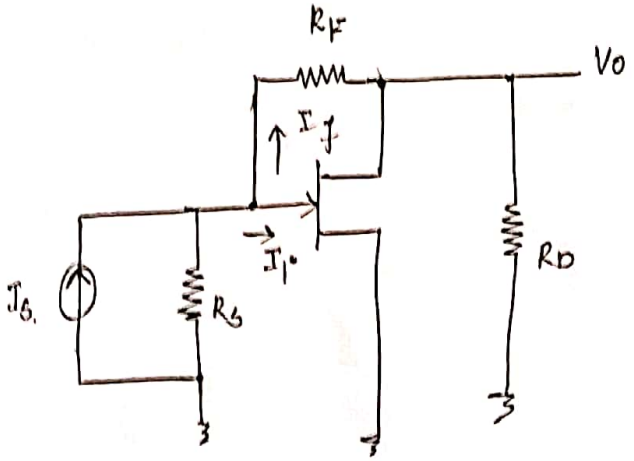
$$A_f = \frac{V_o}{I_s} = \frac{V_o}{I_i} = \frac{A}{1 + A\beta} = \frac{1}{\beta} = -R_0$$

$$A_{vf} = \frac{V_o}{I_s} \times \frac{I_s}{V_i} = -R_0 (1/R_1) = -R_0/R_1$$

using the FET amplifier in Vfg shunt feedback with no feedback $V_f = 0$

$$A = \frac{V_o}{I_i} = -g_m R_D R_S$$




Vfg shunt feedback Amplifier and Equivalent Circuit

The feedback is $\beta = \frac{I_f}{V_o} = \frac{-1}{R_F}$

With feedback the gain of the circuit is

$$A_f = \frac{V_o}{I_S} = \frac{A}{1+A\beta} = \frac{-g_m R_D R_S}{1+(-1/R_F)(-g_m R_D R_S)}$$

$$= \frac{-g_m R_D R_S}{\frac{R_F + g_m R_D R_S}{R_F}}$$

$$A_f = \frac{-g_m R_D R_S R_F}{R_F + g_m R_D R_S}$$

The voltage gain of the circuit with feedback is then

$$A_{vf} = \frac{V_o}{I_S} \times \frac{I_S}{V_S} = \frac{-g_m R_D R_S R_F}{R_F + g_m R_D R_S}\left(\frac{1}{R_S}\right)$$

$$A_{vf} = \frac{-g_m R_D R_F}{R_F + g_m R_D R_S}$$

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# Oscillators and its operation

Oscillators are employed to produce sinusoidal signals that are used as carriers in radio and television broadcasts. oscillators are also used to produce the square wave used as clocks in computer and other synchronous systems.

oscillator is a device which generates the sinusoidal oscillations without any external input. To generate the oscillations it requires an amplifier and a feedback network & the feedback is of positive feedback

Feedback: The process of injecting a fraction of output back to the input is known as feed back.

Positive feedback: When the feedback signal is in phase with the input signal it is called as positive feedback & amplifier is called feedback amplifier.

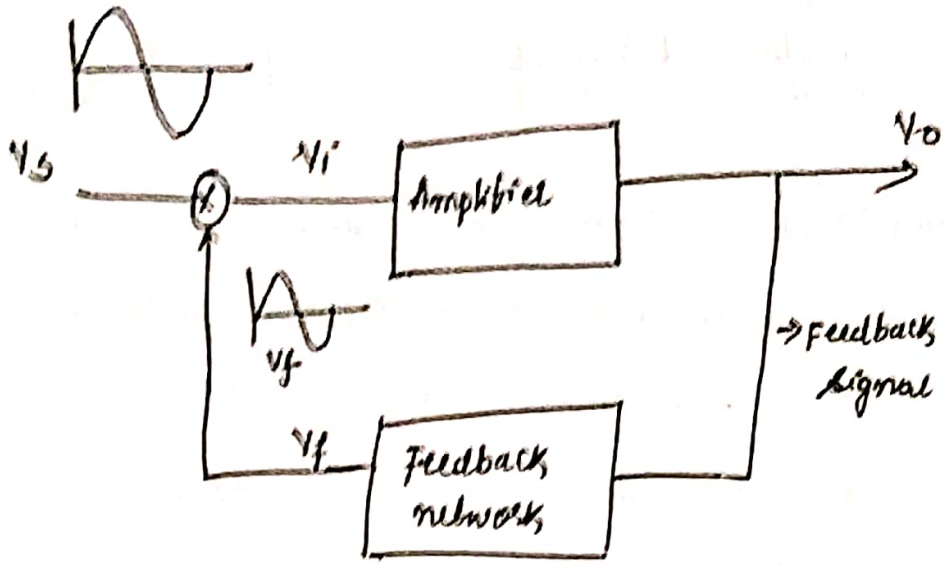
Negative feedback: when the feedback signal is out of phase with the input signal it is called negative feedback

Concept of positive feedback Consider the non-inverting amplifier with the voltage gain A. Since the amplifier is non-inverting the output voltage $V_o$ is in phase with the i/p $V_s$ ($0°$ phase shift) the part of the output is feedback to the input with the help of a feedback network how much part of the output is to be feedback will be decided by the feedback network gain $\beta$.

The amplifier gain $A_{V_1}$ is

$$A_V = \frac{V_o}{V_i}$$

This is called open loop gain of the amplifier.




The Amplifier gain A is given by

$$A = \frac{V_o}{V_i}$$

The gain of the amplifier with feedback is given by

$$\boxed{A_f = \frac{V_o}{V_s}}$$

This is called the closed loop gain of the amplifier.

From the figure WKT the feedback is positive the voltage $V_f$ is added to $V_o$ to generate i/p of amplifier $V_i$

$$\boxed{V_i = V_s + V_f}$$

The feedback n/w gain is

$$\beta = \frac{V_f}{V_o}$$

$$\boxed{V_f = \beta V_o}$$

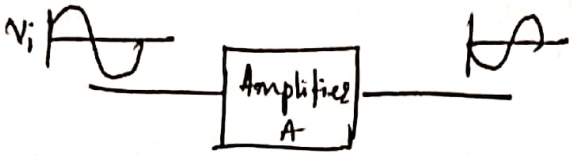
Therefore $V_i = V_s + V_f$

$V_i = V_s + \beta V_o$ WKT $V_o = AV_i$

$V_i = V_s + AV_i\beta$

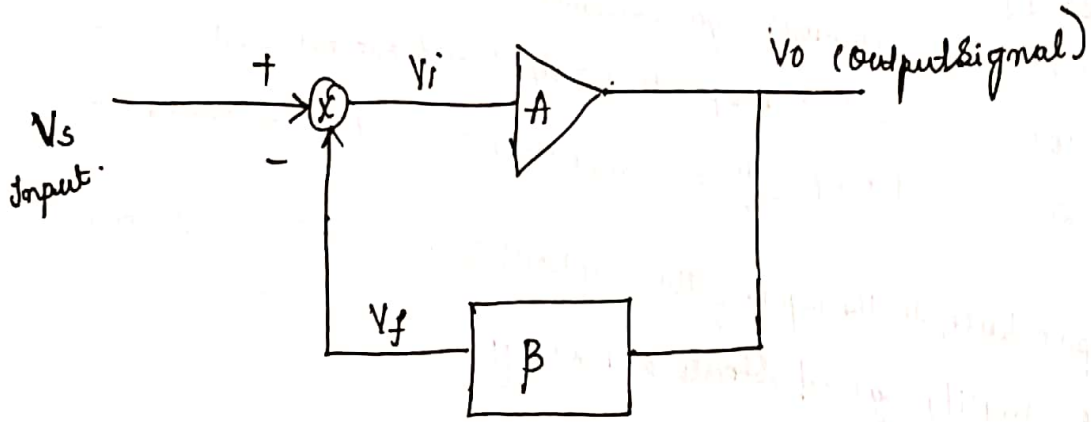
$V_s = V_i - A\beta V_i$

Consider the basic inverting amplifier with an open loop gain A. The feedback network attenuation factor $\beta$ is less than unity. As basic amplifier is inverting it produces a phase shift of 180° b/w input and output.




Inverting amplifier.

For an oscillator the feedback must be positive i.e voltage $V_f$ must be in phase with $V_i$. Thus the feedback network must introduce phase shift of 180°. This ensures the positive feedback.




Basic Block diagram of oscillator circuit.

Let $V_i$ be the input voltage at the amplifier i/p then $\boxed{V_o = A V_i}$ $\left(\because A = \frac{V_o}{V_i}\right)$ is the output voltage of the amplifier.

& $\boxed{V_f = \beta V_o}$ $\left(\because \beta = \frac{V_f}{V_o}\right)$ the feedback voltage.

$A\beta$ is refered to as the loop gain.

WKT $\beta = \frac{V_f}{V_o} \Rightarrow V_f = \beta V_o$

$\Rightarrow V_f = \beta \times A V_i$

$A_f = \frac{A}{1 - A\beta}$

For an oscillator the feedback network drives the amplifier i.e $V_f$ acts as $V_i$

so $V_f = V_i$

$$V_s = V_i(1-A\beta)$$

$$A_f = \frac{V_o}{V_s} = \frac{V_o}{V_i(1-A\beta)}$$

WKT $\frac{V_o}{V_i} = A$

$$\boxed{A_f = \frac{A}{1-A\beta}}$$

Now consider the various values of $\beta$ and the corresponding values of $A_f$ for constant amplifier gain of A of 20 $\boxed{A=20}$

| A | $\beta$ | $A_f$ |
|---|---|---|
| 20 | 0.005 | 22.22 |
| 20 | 0.004 | 100 |
| 20 | 0.0045 | 200 |
| 20 | 0.05 | $\infty$ |

Conclusion: From the table it is shown that the gain with feedback increases as the amount of positive feedback increases & gain becomes infinite. This indicates that Circuit can produce output without External i/p $V_s=0$ i.e $A_f = \frac{V_o}{V_s} = \infty$ means $V_s=0$ Just by feeding the part of the output back to the input of the amplifier circuit. In this Condition the circuit stops amplifying and starts oscillating.

## Barkhausen Criterion

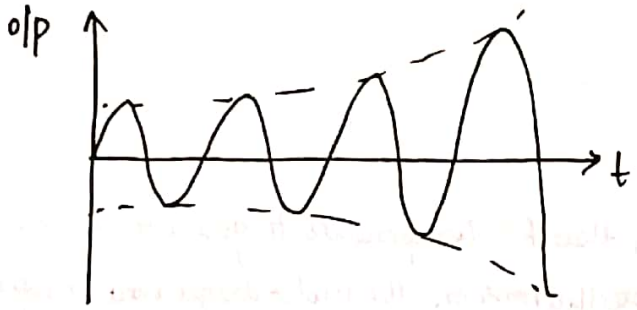
Barkhausen criterion states that

① The total phase shift around a loop as the signal proceeds from i/p Through amplifier & the feedback network back to i/p again completing a loop is 0° or 360° ( for inverting amplifier total phase shift around a loop is 360° & for non-inverting amplifier total phase around a loop is 0°)

② The magnitude of the product of the open loop gain of the amplifier (A) & the magnitude of the feedback factor $\beta$ is unity i.e loop gain $|A\beta| = 1$

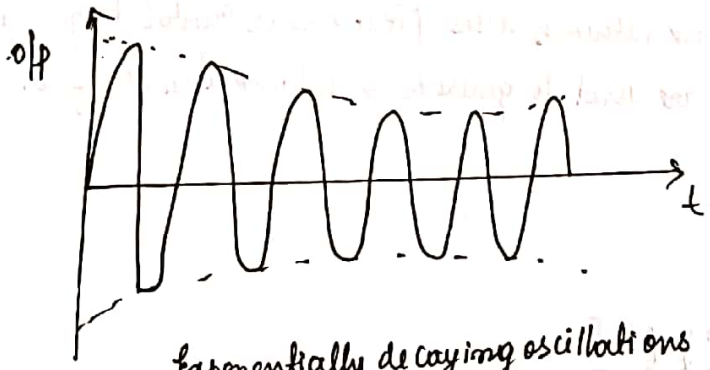
From the oscillator circuit it is observed that the amplifier ckt introduces 180° phase shift and feedback network introduces 180° phase shift so that total phase shift around a loop is 360°. This ensures positive feedback. The two conditions are referred as Barkhausen criteria for oscillator.

$|A\beta| > 1$ & the total phase shift around a loop is 0° or 360° then the output oscillates but the oscillations are of growing type



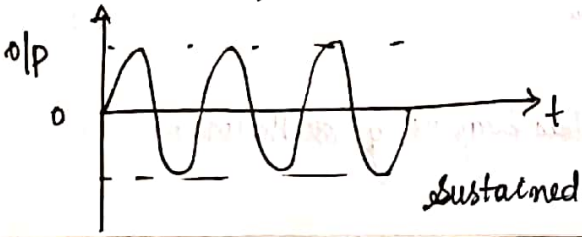

Growing type of oscillations.

$|A\beta| < 1$ & when the total phase shift around a loop is 0 or 360 then the oscillations are decaying type i.e amplitude decreases exponentially & the oscillations are finally cease




Exponentially decaying oscillations

$|A\beta = 1|$ when the total phase around a loop is 0° or 360° then the circuit produces oscillations with constant frequency and amplitude called sustained oscillations




Sustained oscillations.

Note: For the positive feedback the feedback signal should be in phase with the input signal.

## Classification of oscillators

Based on the elements used in feedback network oscillators are classified as follows

1. RC oscillator
2. LC oscillator
3. Crystal oscillator

* In RC oscillators the feedback network uses RC components to generate oscillations RC oscillators are used to generate oscillations in the audio frequency range (20 Hz - 20 KHz)

* In LC oscillator the feedback network employs the LC components to generate oscillations LC oscillators are used to generate oscillations in radio frequency range (100 KHz - 100 MHz)

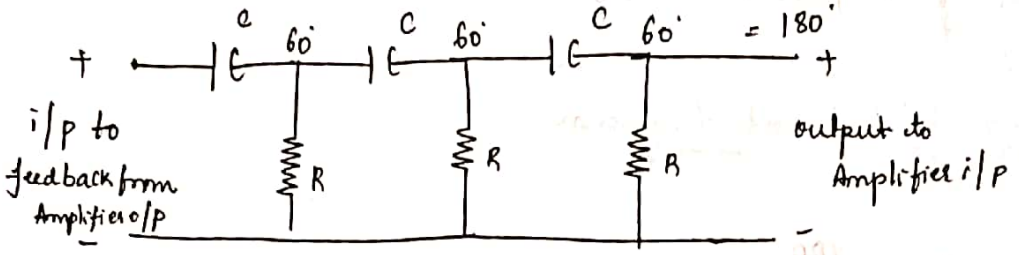
* In Crystal oscillators the feedback network uses piezo electric crystal to generate oscillation. Crystal oscillators are used to generate oscillations in the frequency range of (10 KHz - 10 MHz)

## RC phase Shift oscillator using FET

- In RC phase shift oscillator RC network is used in feedback path. In oscillator feedback network must introduced phase shift of 180° to obtain the total phase shift around a loop as 360 or 0°

* RC phase shift oscillator is a low frequency oscillator.

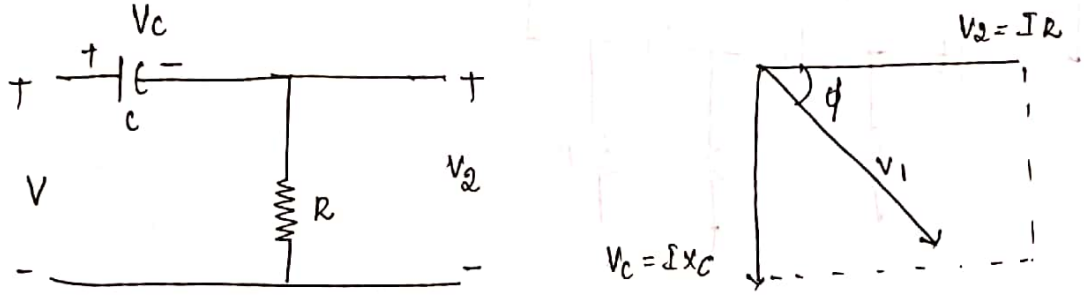
## RC feedback network




Feedback network in Rc phase shift oscillator.

one Rc Network produces phase shift of 60° Then to produce phase shift of 180° the network are connected in series to generate total phase of 180° The n/w is designed in such a way that all the resistance values and Capacitance values are same so that for particular frequency each section of R & C produces a phase shift of 60°.

Consider the single Rc network




Single Rc Network and phasor diagram.

The resistor voltage and current are in phase & in a capacitor the current leads the voltage by an angle 90°. $V_1$ & $V_2$ differ in phase by angle $\phi$

$$\tan\phi = \frac{V_c}{V_2} = \frac{I X_C}{I R} = \frac{X_C}{R}$$

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C}$$

$$\tan\phi = \frac{1}{2\pi f RC}$$

The values of R & C are selected so as to give a phase shift of 60° at the desired

frequency of oscillations. Since all the three RC sections are identical the total phase shift introduced by the feedback network is 180°.

FET phase shift oscillator : CKt diagram

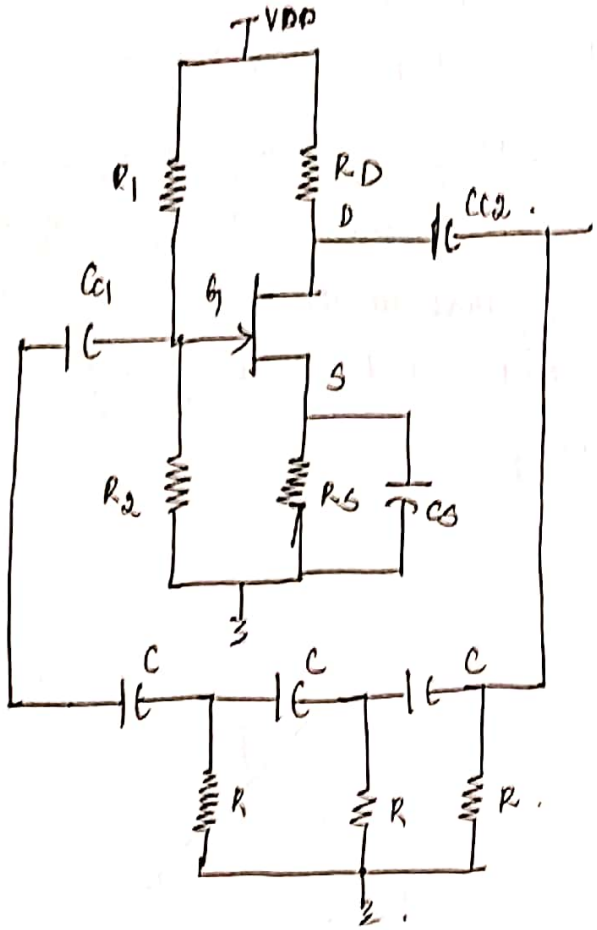
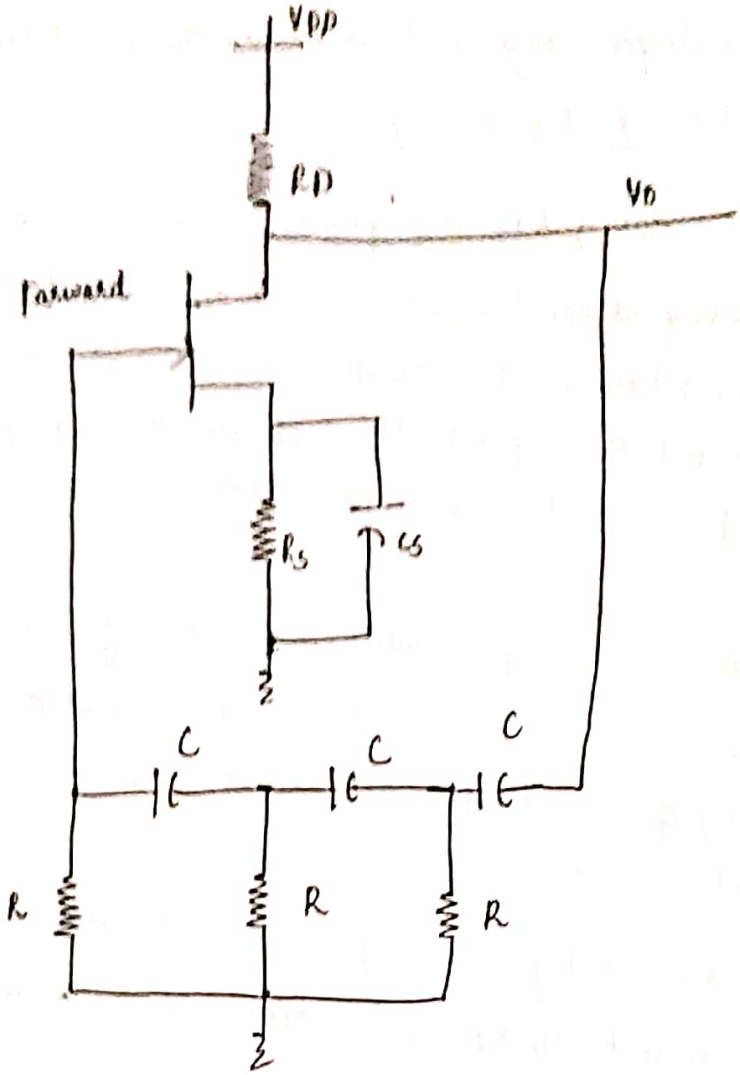
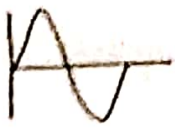



Figure shows the circuit of FET RC phase shift oscillator. It consists of single stage amplifier and a feedback network comprising of three identical RC sections.

The resistors $R_1$ and $R_2$, $R_S$ provides the necessary bias to the amplifier circuit.

If the output voltage of the feedback network were directly connected to the amplifier input the relatively low input resistance of the amplifier input the relatively low i/p resistance of the amplifier appreciably loads down the feedback network, therefore voltage shunt is used.



For the amplifier stage FET is used. It is self biased with a capacitor bypassed Source resistance $R_S$ and drain bias resistance $R_D$.

The parameters of FET are $g_m$ and $r_d$

$$|A| = g_m R_L$$

$$R_L = R_D \| r_d$$

The feedback n/w is again in 3-stage $R_C$ n/w having gain

$$\beta = 1/29$$

$$|A| \geq 29.$$

The frequency of oscillation is given by

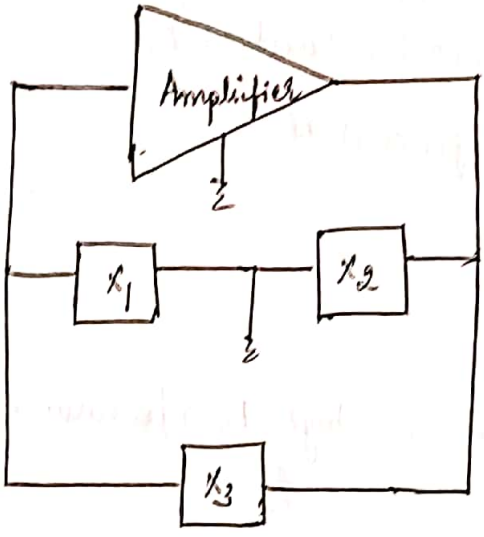
$$f = \frac{1}{2\pi RC\sqrt{6}}$$

Advantages: The circuit is simple to design and can produce the output over the audio frequency range. It is a fixed frequency oscillator.

Drawbacks: By changing the value of R & C the frequency of the oscillator can be changed but the value of R & C of all the three sections must be changed. The value of R & C of all the three sections must be changed simultaneously to satisfy the oscillating conditions. But this is practically impossible. Hence the phase oscillator is considered as a fixed frequency oscillator.

LC oscillators: LC oscillators employs parallel LC circuit to generate sinusoidal oscillations. parallel LC circuit is also called as tuned circuit or resonant circuit. The frequency of oscillations is determined from the resonant condition of the tuned circuit.

Figure below shows the basic configurations of LC oscillator. Based on the nature of the reactive element $X_1$, $X_2$, $X_3$ two types of LC oscillators can be obtained.



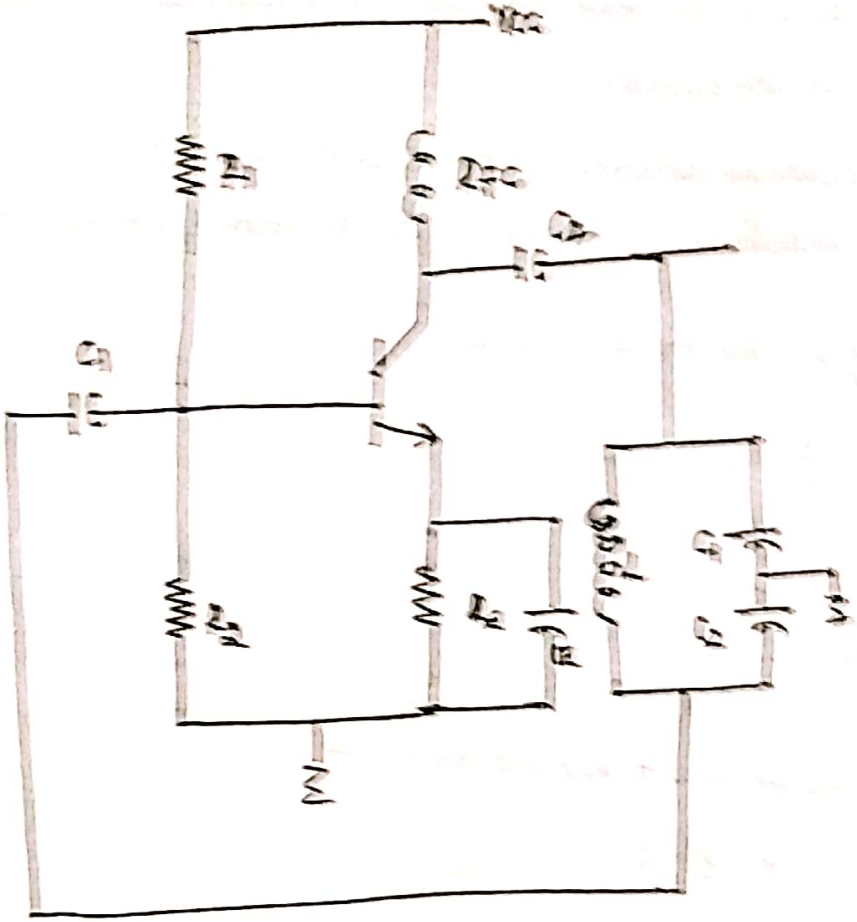

LC oscillators are classified into two types.

① Transistor hartley oscillator.

② Transistor colpitts oscillator.

## Transistor Colpitts oscillator

Figure shows the transistor Colpitts oscillator. It consists of a CE amplifier which introduces a phase shift of 180°. Resistors $R_1$ and $R_2$ are used to establish the desired operating point.




The feedback network consists of a tapped capacitive voltage divider $C_1$ & $C_2$ in parallel with the inductor L. The voltage across $C_2$ is fed back to the amplifier input through the coupling capacitor $C_c$.

If choke is a large inductor its function of choke is

(1) It acts as a dc short to the power supply Vcc it allows the dc current easily to pass through.

(2) It acts as an open circuit for ac

RFC choke is used to achieve the isolation between ac and dc.

* when the supply voltage is provided the oscillatory current is setup in the tank circuit. It produces ac voltages across $C_1$ and $C_2$. tank circuit provides the 180° phase shift. The total phase shift around the loop is 360°.

The output is coupled to the load through a transformer. transformer coupling has the following advantages

1. It provides electrical isolation b/w the oscillator o/p & load
2. It provides impedance matching b/w the oscillator o/p & the load.

The frequency of oscillations is given by

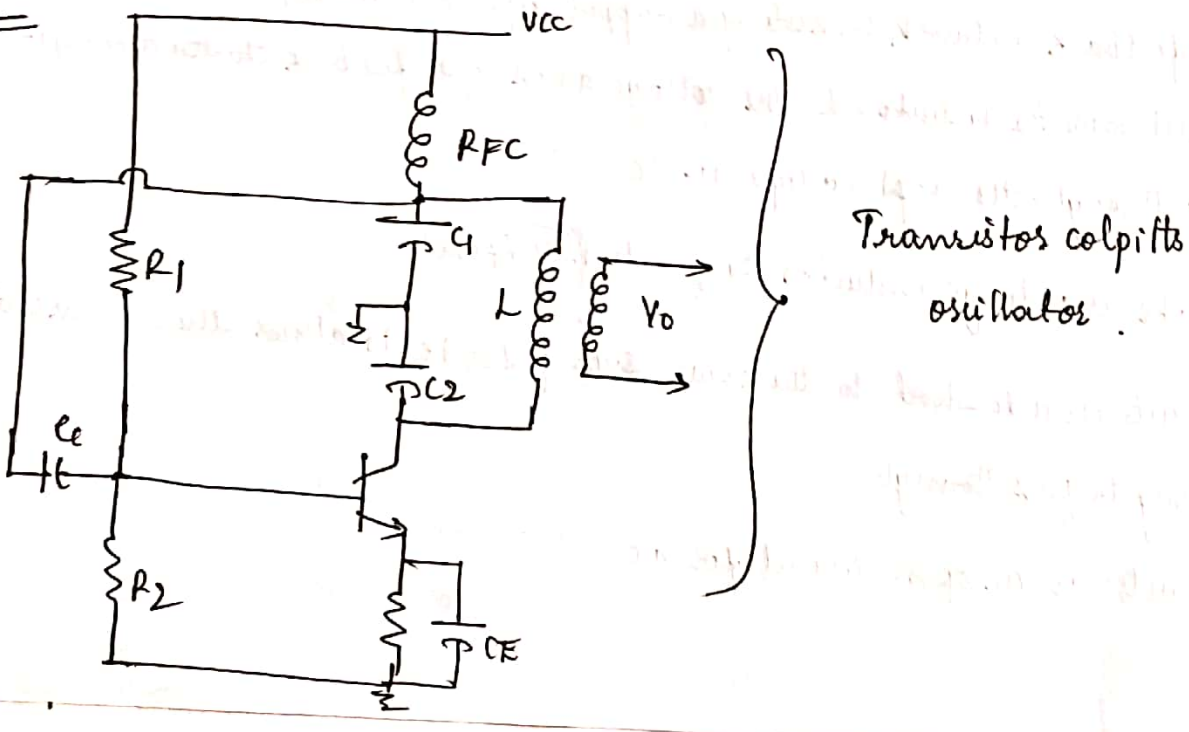
$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

The condition for sustained oscillation is

$$h_{fe} \geq C_2/C_1$$

(or)




Transistor colpitts oscillator.

# Transistor hartley oscillator

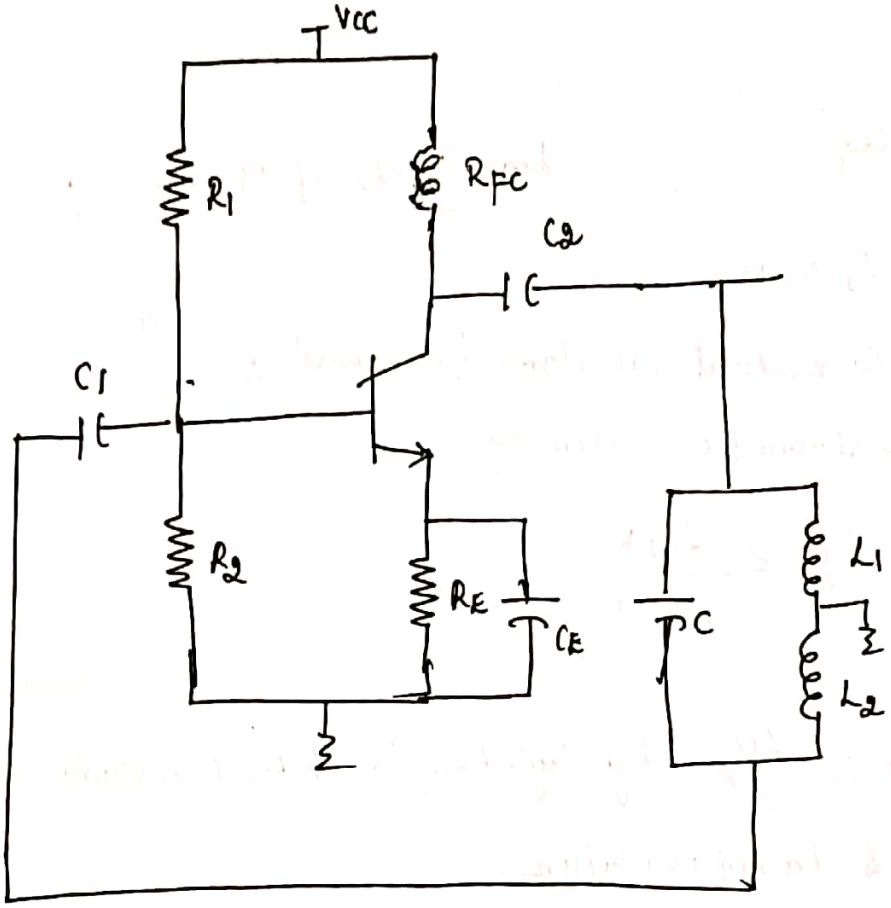



Figure shows the transistor hartley oscillator. It consists of a CE amplifier which introduces a phase shift of 180°. Resistors $R_1$, $R_2$, $R_E$ used to establish the desired operating point.

The fed network consists of tapped inductive voltage devider $L_1$ and $L_2$ in parallel with the capacitor C. The voltage across $L_1$ is fed back to the amplifier input through the coupling capacitor $C_c$

$R_F$ choke is a large inductor the function of $R_{FC}$ choke is

① It acts as a dc short to the power supply Vcc i.e it allows the dc current easily to pass through.

② It acts as an open circuit for ac

The capacitor $C_1$ creates the ground at the junction of $L_1$ and $L_2$. The phase at the tank circuit is 180° and the total phase around the loop is 360°.

The frequency of oscillations is given by

$$f = \frac{1}{2\pi\sqrt{L_{eq}C}}$$

$L_{eq} = L_1 + L_2$ if M is not given.

$L_{eq} = L_1 + L_2 + 2M$

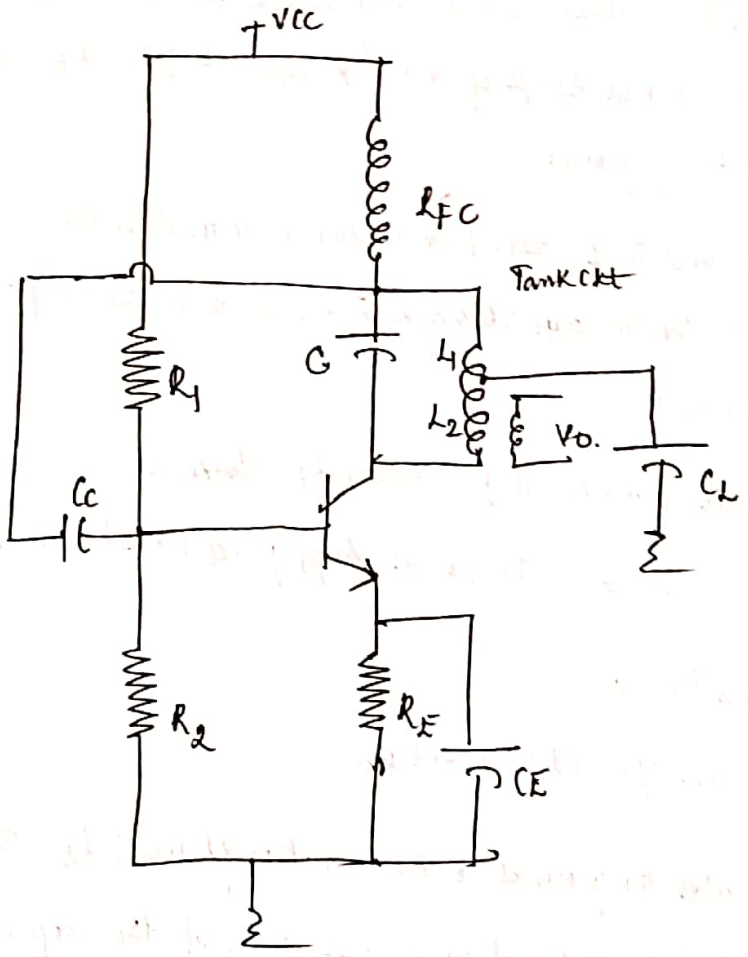
where M is the mutual inductance b/w $L_1$ and $L_2$.

the condition for sustained oscillation is

$$h_{fe} \geq \frac{L_1 + M}{L_2 + M}.$$

$h_f \geq L_1/L_2$ by Neglecting the Mutual Inductance this is the condition for sustained oscillations.

Q.

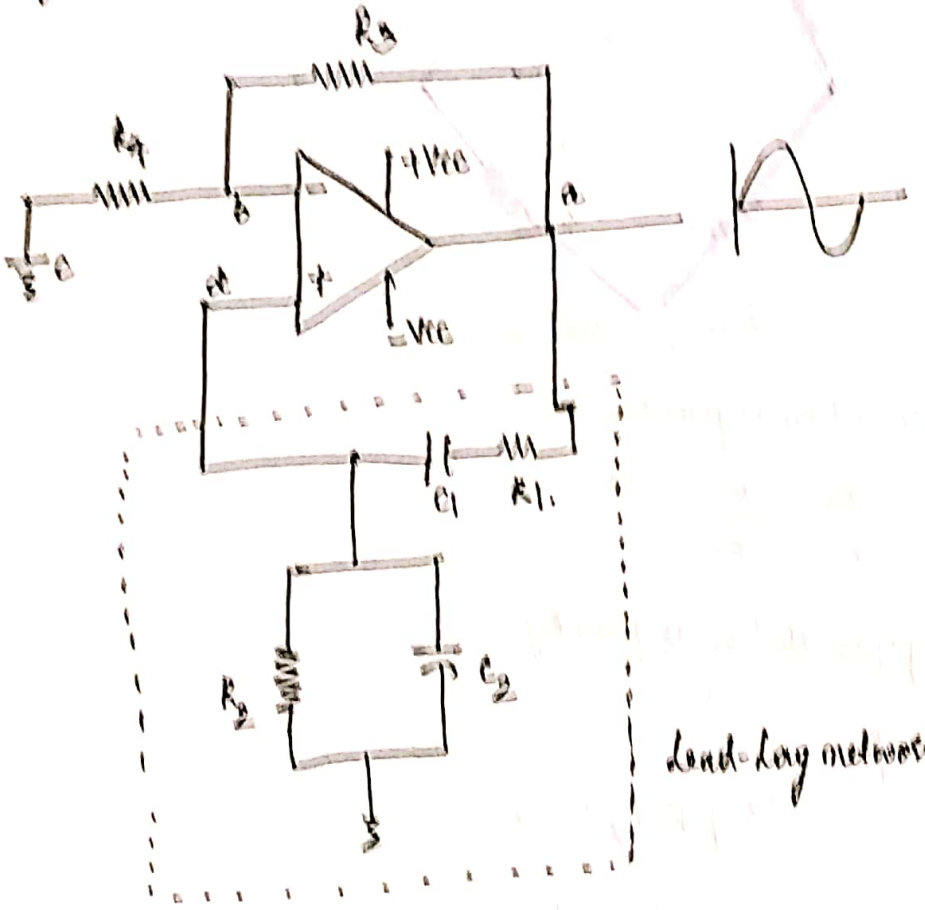


## Wien Bridge oscillator

Wien bridge oscillator is one of the oscillator circuit is used to generate sinusoidal oscillations in the audio frequency range.

Figure below shows the circuit of wien bridge oscillator.

- It consists of an op-amp with inverting amplifier in the feedback path and lag network in the feedback path.
- $R_3$ & $R_4$ resistors are a fixed resistors which parallel $R_2$ & $C_2$ networks is the lag network.
- The feedback resistors $R_3$ & $R_4$ of op-amp amplifier and lead & lag network forms a bridge circuit it is called as wien bridge oscillator.

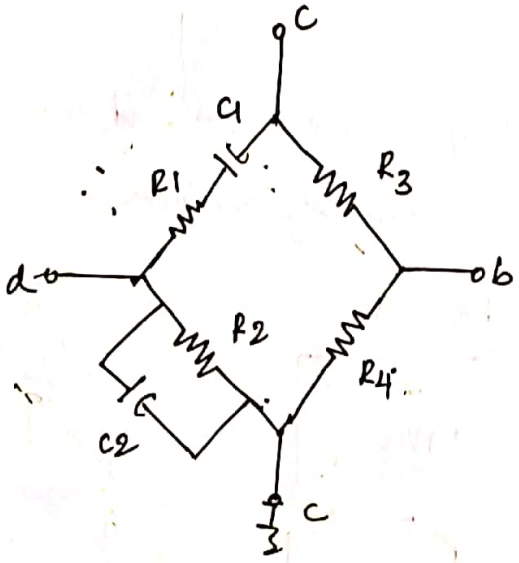



Wein bridge oscillators using op-amp amplifier.

At the oscillator frequency the lead lag network is designed to introduce Zero degree phase shift.

The op-amp non-inverting amplifier introduces Zero degree phase shift hence the total phase shift around the loop is Zero

The expression for the frequency of oscillation is obtained from the balancing condition of the bridge




Bridge circuit.

The balancing condition is given by

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1}$$

The frequency of oscillation is given by

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

If $R_1 = R_2 = R$ & $C_1 = C_2 = C$ then

$$f = \frac{1}{2\pi RC}$$

For Sustained oscillation the gain of the amplifier should be atleast equal to 3

$$1 + \frac{R_3}{R_4} \geq 3$$

$$\frac{R_3}{R_4} \geq 2.$$

## Crystal oscillator

It is basically a tuned circuit oscillator the circuit design is similar to colpitts oscillator it uses a piezo electric crystal instead of an inductor Crystal oscillators are used in communication transmitters and receivers where high frequency stability is required.

## Piezo Electric Effect

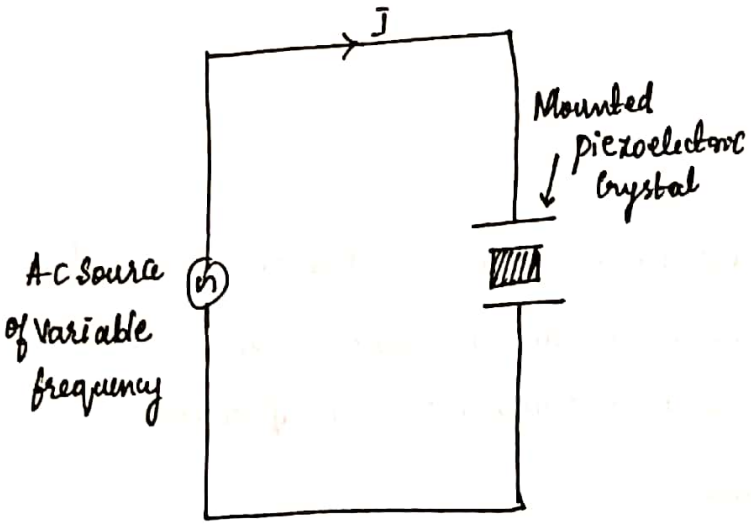
Piezo - Electric Effect is an electromechanical phenomenon. If the crystal is mechanically vibrated it develops an AC voltage across the ends of the crystal The Resonant frequency of the crystal is inversly proportional to the thickness of the crystal. the frequency of oscillations increases as the thickness of the crystal decreases

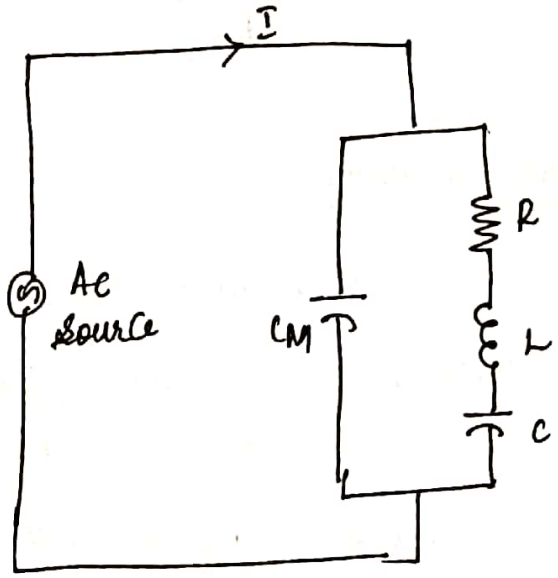
## characteristics of quartz crystals.

The quartz crystals are the best choice in sinusoidal oscillators due to the following reasons.

1. They are mechanically strong
2. They have good piezoelectric sensitivity
3. They are less expensive.

Figure shows the piezoelectric crystal mounted between the plates and connected across an AC source of variable frequency & another figure shows the electrical equivalent circuit of the mechanically vibrating crystal.



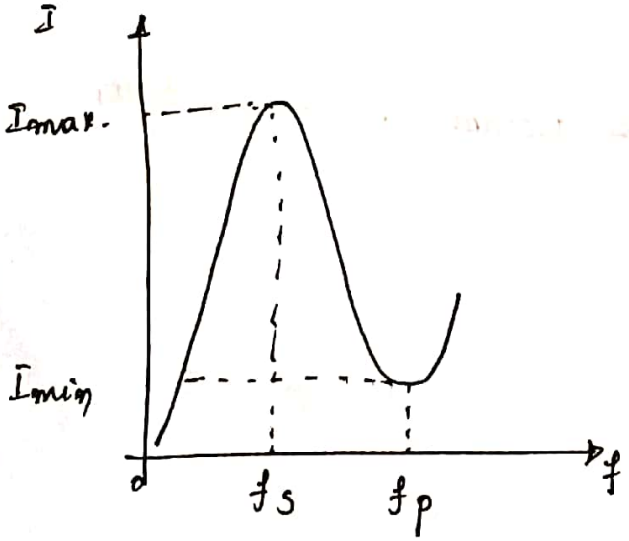

L – Electrical equivalent inductance of crystal mass

C – Electrical equivalent capacitance of the crystal compliance

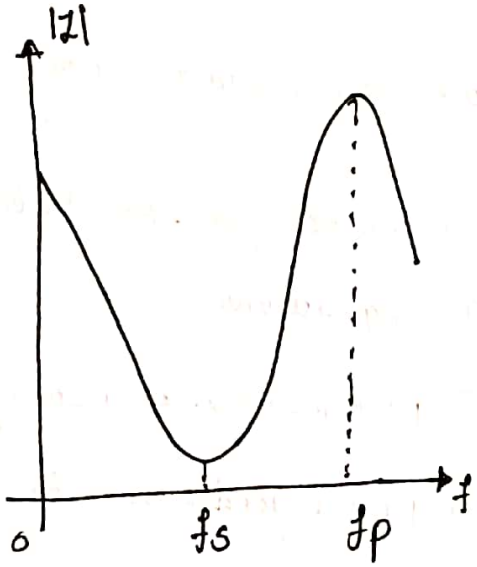
R – Electrical equivalent resistance of the crystal structure's internal friction

$C_M$ – Capacitance due to mechanical mounting of the crystal.

The frequency response of the crystal is obtained by plotting the current I through the crystal as a function of the frequency of ac source.




Frequency response of piezoelectric Crystal




Crystal impedance versus frequency

when the frequency of the ac source is equal to the frequency $f_s$ the current through the crystal becomes maximum ($I_{max}$). This condition is called the series resonance and $f_s$ is called the series resonant frequency. Series resonance occurs when the reactance of L is equal to the reactance of C in series RLC branch.

$$\omega L = \frac{1}{\omega C}$$

$$\omega^2 = \frac{1}{LC}$$

$$\omega = \frac{1}{\sqrt{LC}}$$

$$f = f_s = \frac{1}{2\pi\sqrt{LC}}$$

Since the current is maximum the impedance of the crystal is minimum. when the frequency of ac source is equal to the frequency $f_p > f_s$ the current through the crystal becomes minimum ($I_{min}$). This condition is called parallel resonance and $f_p$ is called the parallel resonant frequency.
Parallel resonance occurs when the reactance of L is equal to the sum of the reactances of $C_M$ & C

$$\omega L = \frac{1}{\omega C_M} + \frac{1}{\omega C}$$

$$\omega^2 = \frac{1}{L}\left[\frac{1}{C_M} + \frac{1}{C}\right]$$

$$\frac{1}{C_p} = \frac{1}{C_M} + \frac{1}{C}$$

$$\frac{1}{C_p} = \frac{C + C_M}{C C_M}$$

$$C_p = \frac{C_M C}{C_M + C}$$

$$\omega^2 = \frac{1}{LC_p} = \frac{1}{\sqrt{LC_p}}$$

$$f = f_p = \frac{1}{2\pi\sqrt{LC_p}}$$

Since the current is minimum the impedance of the crystal is maximum

To Show that $f_s = f_p$

W.K.T $$\frac{1}{C_p} = \frac{1}{C} + \frac{1}{C_M}$$

$$C_M >> C$$

$$\frac{1}{C_M} << \frac{1}{C}$$

Neglect $\frac{1}{C_M}$

$$\frac{1}{C_p} \simeq \frac{1}{C}$$

$$\therefore C_p = C$$

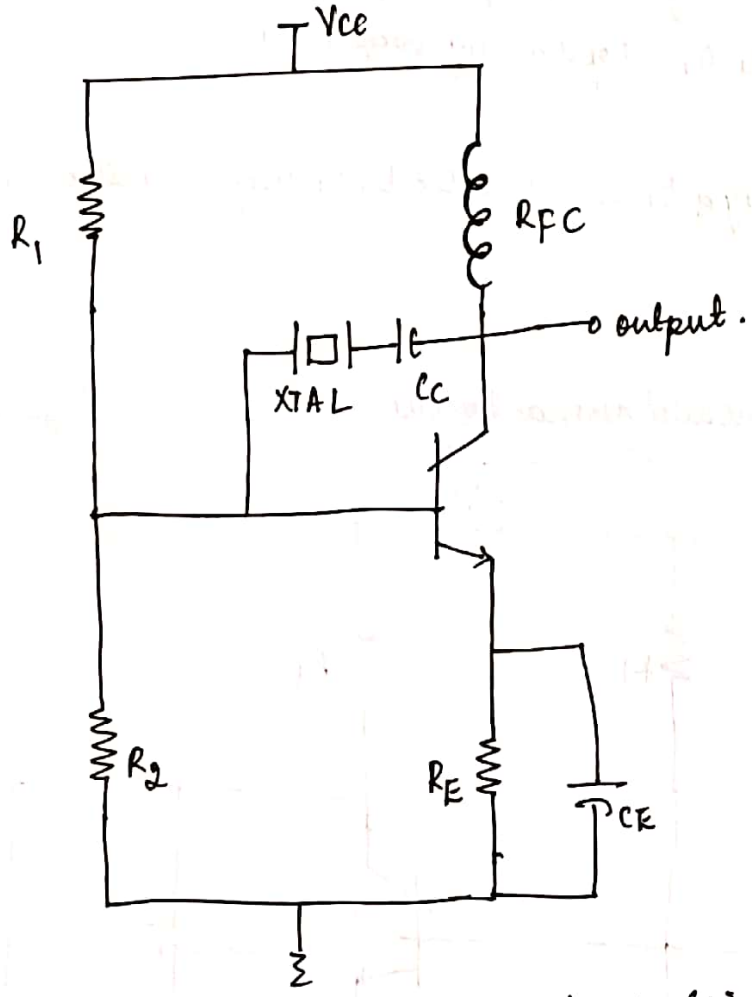
$$\boxed{f_p = \frac{1}{2\pi\sqrt{LC}}}$$

## Transistor Crystal oscillator

The Crystal can be operated either in the Series resonant mode or in the parallel resonant mode

## Crystal oscillator in Series resonant mode

Figure shows the circuit of Crystal oscillator in which Crystal is operated in Series resonant mode.




Transistor Crystal oscillator operating in Series resonant mode

* The circuit uses a transistor CE Stage $R_1$, $R_2$ & $R_E$ are selected to establish the desired Q-point, $C_E$ bypasses the emitter resistor $R_E$
* The coupling capacitor $C_C$ is selected such that it acts as a short circuit at the oscillator frequency

* $R_{FC}$ acts as a short for dc current and open circuit for ac signal.

* Crystal is used as series element in the feedback path so that it operates in series resonant mode. Crystal has minimum impedance at the series resonant frequency $f_s$ therefore maximum feedback from collector to base occurs at this frequency

* once the oscillations are setup the frequency of oscillations is held stabilized at $f_s$ by the crystal. Changes in supply voltage, transistor device parameters have no effect on the circuit operating frequency.

* The frequency stability of the circuit is set by the frequency stability of the crystal which is very high.

## Crystal oscillator in parallel resonant mode

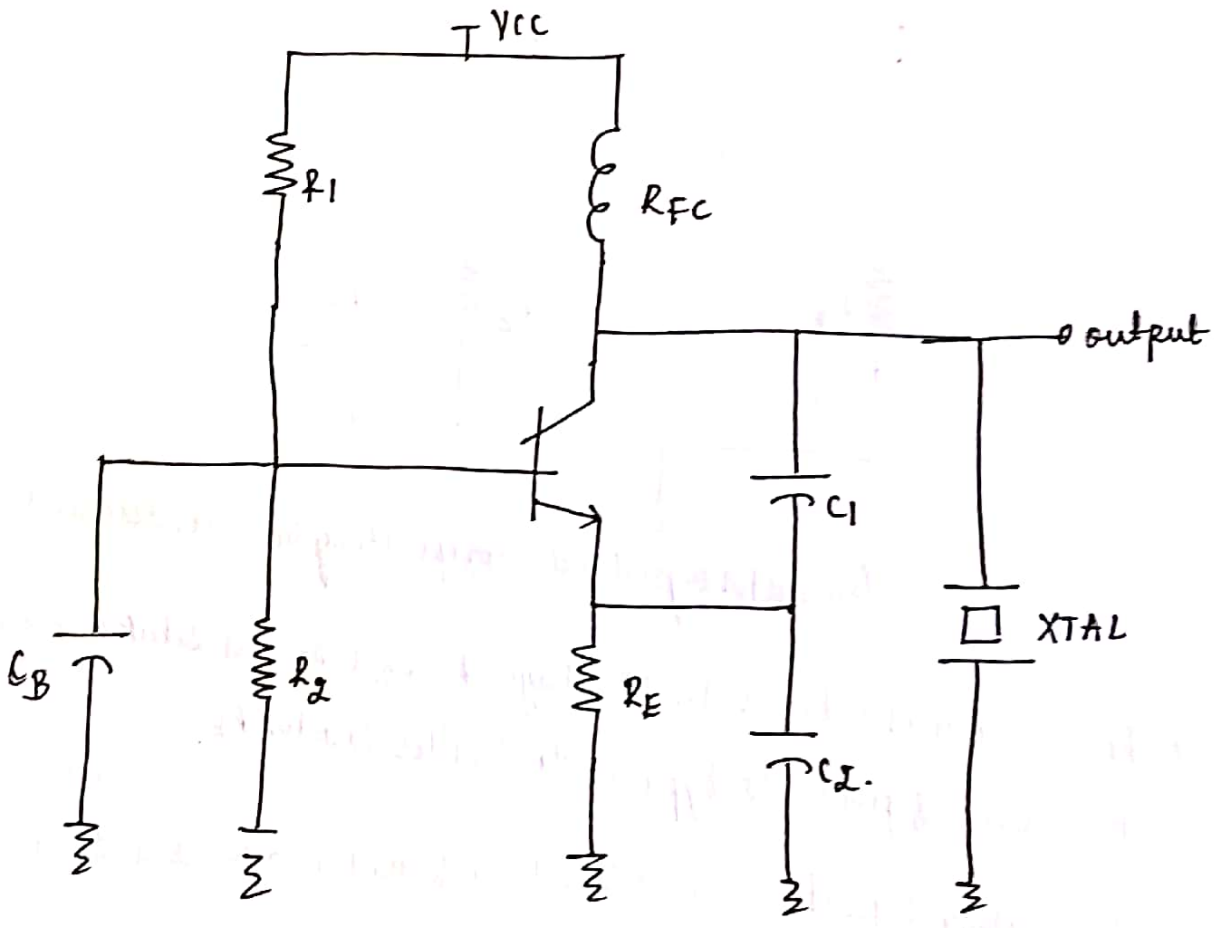


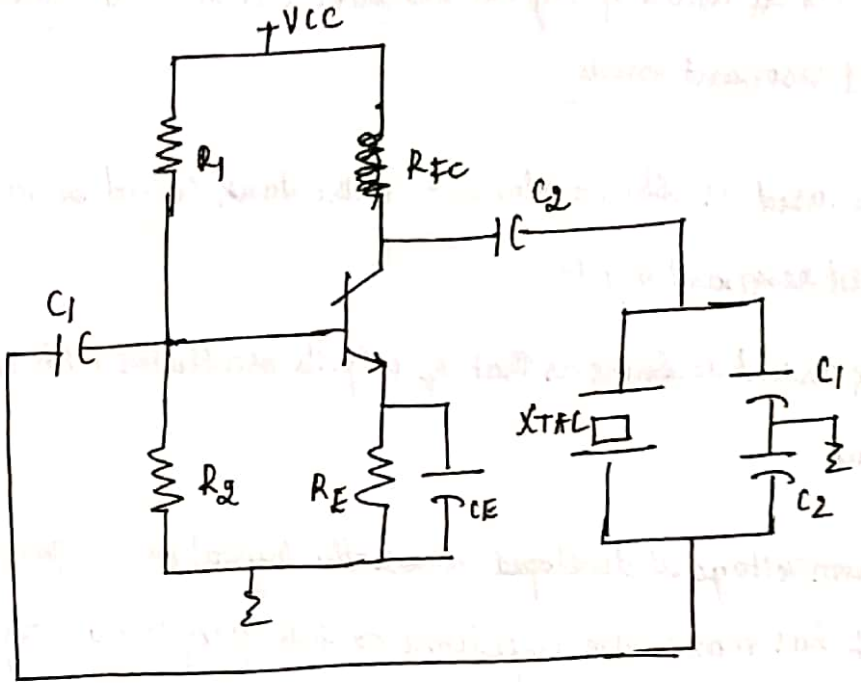
Figure shows the circuit of crystal oscillator in which the crystal is operated in its parallel resonant mode

- Crystal is used as shunt element in the tank circuit so that it operates in parallel resonant mode
- The tank circuit is same as that of colpitts oscillator with inductor replaced by a crystal
- Maximum voltage is developed across the crystal at its parallel resonant frequency since it has maximum impedance at this frequency. Crystal behaves as inductance at parallel resonant frequency
- The oscillations are sustained at the parallel resonant frequency $f_p$. Series combination of $C_1$ and $C_2$ acts as a voltage divider for the output voltage
- The voltage across $C_2$ is fed to the emitter of the transistor the feedback voltage is maximum at the parallel resonant frequency of the crystal.
- $C_E$ is the bypass capacitor which acts as a short circuit at the oscillator frequency bypassing it around the bias.

Applications of crystal oscillator

1) To provide the clock signal for computers and other synchronous digital systems
2) To provide carrier frequency in communication transmitters.
3) To provide the local oscillator frequency in communication receivers

Transistor BJT Crystal oscillator with feedback.




→ Colpitts oscillator can by modified by using the Crystal to behave as an ~~oscillator~~ inductor.

→ The Crystal behaves as an inductor for a frequency slightly higher than the Series resonance frequency $f_S$

→ The two capacitors connected in parallel with XTAL.

→ $R_1, R_2, R_E$ provides the necessary biasing condition

→ $R_{FC}$ is used for isolation of ac to dc.

→ Frequency of oscillation

$$f = \frac{1}{2\pi\sqrt{LC}}$$

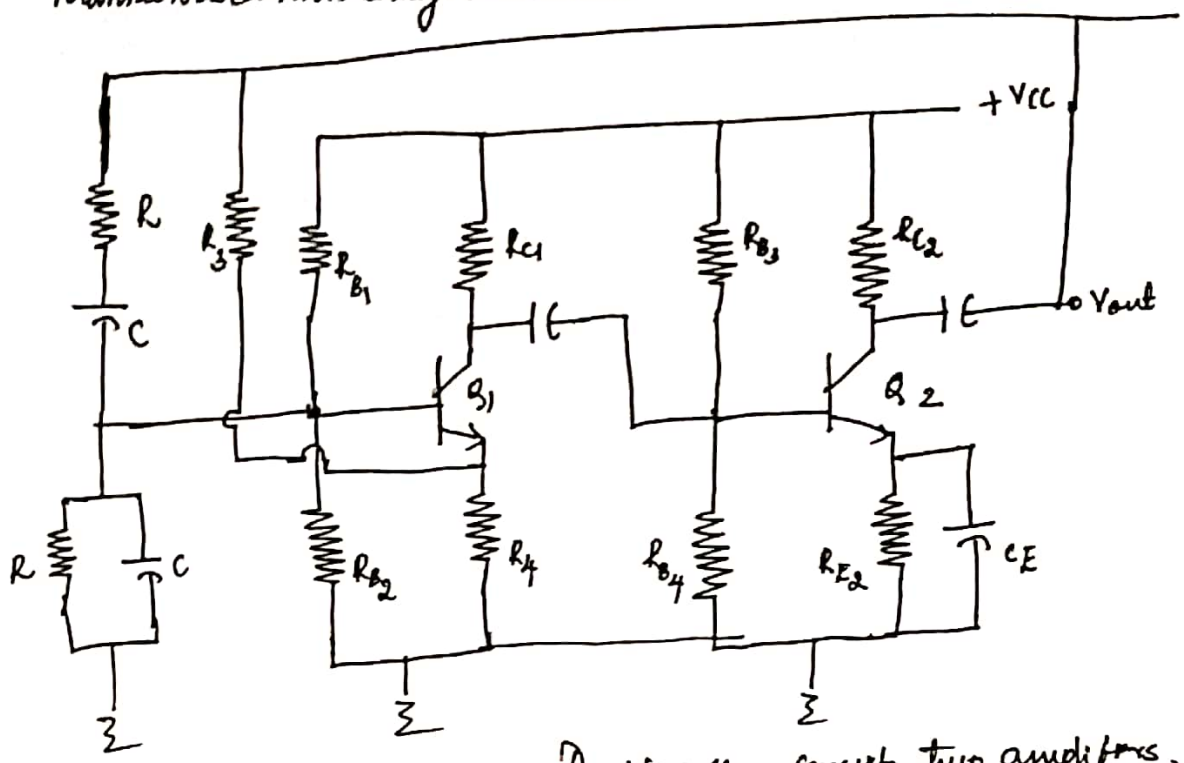
amplifier phase shift 180° &
feedback n/w phase 180° total
loop phase is 360°

Parallel resonance frequency

$$C_{eq} = \frac{C_M C}{C + C_M}$$

$$f_p = \frac{1}{2\pi\sqrt{L C_{eq}}}$$

Transistorised wien Bridge oscillator.




Amplifier stage consists two amplifiers.

Transistorized wien Bridge oscillator

→ The wein bridge oscillator consists of two stage common Emitter transistor amplifiers

→ Each stage contributes 180° phase shift hence the total phase shift due to the amplifier stage becomes 360° or 0° which is necessary as per the oscillator conditions

→ The Bridge consists of $R_1$ & $C_1$ in series, $R_2$ & $C_2$ in parallel. $R_3$ & $R_4$

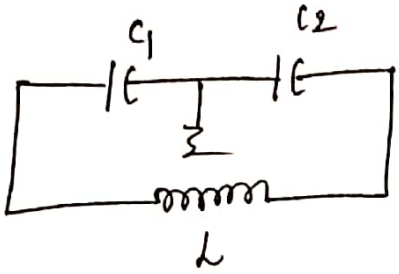
→ The feedback is applied from the collector of $Q_2$ through the coupling capacitor to the bridge circuit.

→ The Resistance $R_4$ serves the dual purpose of Emitter resistance of the transistor $Q_1$ and also the element of wein Bridge

→ The two stage amplifier provides a gain much more than 3 so it is necessary to reduce it.

## Frequency of oscillations for colpitts oscillator.

Consider the tank circuit




Sum of all three reactances should be equal to zero.

$$\frac{1}{jX_{C_1}} + \frac{1}{jX_{C_2}} + jX_L = 0$$

$$-jX_{C_1} - jX_{C_2} + jX_L = 0$$

$$jX_L = j(X_{C_1} + X_{C_2})$$

$$X_L = X_{C_1} + X_{C_2}$$

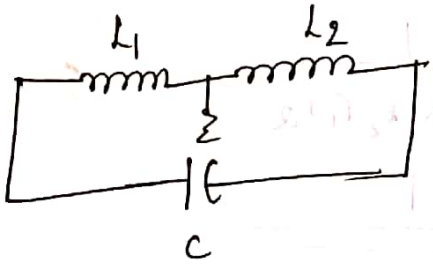
$$\omega L = \frac{1}{\omega C_1} + \frac{1}{\omega C_2} \Rightarrow \omega^2 = \frac{1}{L}\left[\frac{1}{C_1} + \frac{1}{C_2}\right]$$

$$= \frac{1}{L}\left[\frac{C_1 + C_2}{C_1 C_2}\right]$$

$$\omega^2 = \frac{1}{LC_{eq}}$$

$$\boxed{\omega = \frac{1}{2\pi\sqrt{LC_{eq}}}}$$

## Frequency of oscillation for Hartley oscillator.




Sum of all three reactances should be equal to zero.

$$jX_{L_1} + jX_{L_2} + \frac{1}{jX_C} = 0$$

$$j(X_{L_1} + X_{L_2}) = jX_C \Rightarrow \omega L_1 + \omega L_2 = \frac{1}{\omega C} =$$

$$\omega^2(L_1 + L_2) = \frac{1}{C} \Rightarrow \omega^2 = \frac{1}{L_{eq}C}$$

$$L_{eq} = L_1 + L_2$$

$$f = \frac{1}{2\pi\sqrt{L_{eq}C}}$$

# Frequency of oscillation for Wein-Bridge oscillator.

To get sustained oscillation Barkhausen criteria should satisfy $A\beta = 1$

Therefore gain $A_f$ of non-inverting Amplifies

$$A_f = 1 + \frac{R_f}{R_m}$$

$$A_f = 1 + R_3/R_4$$

$$1 + R_3/R_4 \geq 3$$

$$R_3/R_4 \geq 2$$

$$R_3 = \left[ R_1 - \frac{j}{\omega C_1} \right] R_4 \left[ \frac{1}{R_2} + j\omega C_2 \right]$$

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + R_1 j\omega C_2 - \frac{j}{\omega C_1 R_2} - \frac{j^2 \omega C_2}{\omega C_1}$$

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + R_1 j\omega C_2 - \frac{j}{\omega C_1 R_2} + \frac{C_2}{C_1}$$

Equating Real and Imaginary parts.

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1} \qquad R_1 j\omega C_2 = \frac{j}{\omega C_1 R_2}$$

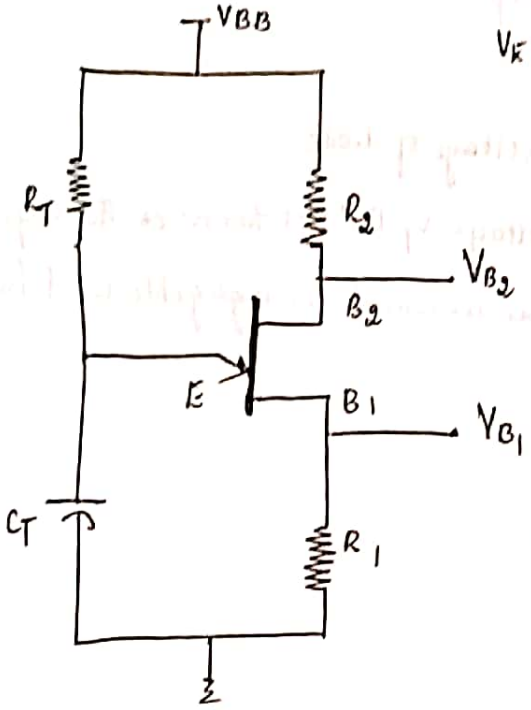
$$\omega^2 = \frac{1}{R_1 R_2 C_1 C_2}$$

$$\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

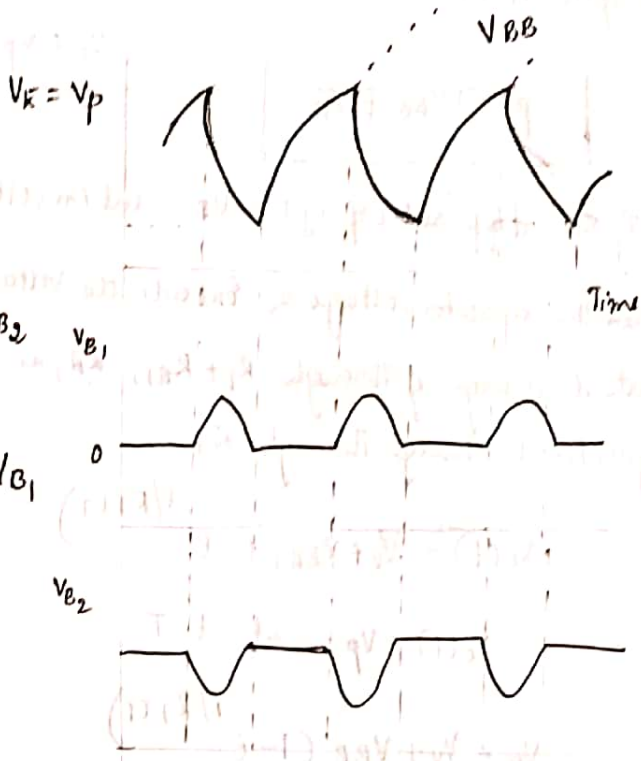
$$\boxed{f = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}}}$$

## unijunction oscillator

unijunction transistor can be used in a single stage oscillator circuit to provide a pulse signal suitable for digital circuit applications. The unijunction transistor can be used in what is called a relaxation oscillator.




Basic unijunction oscillator circuit




unijunction oscillator waveform.

$R_T$ and $C_T$ are the timing components that set the circuit oscillating rate.

The frequency of oscillation is calculated by

$$f_o = \frac{1}{R_T C_T \ln\left(\frac{1}{1-\eta}\right)}$$

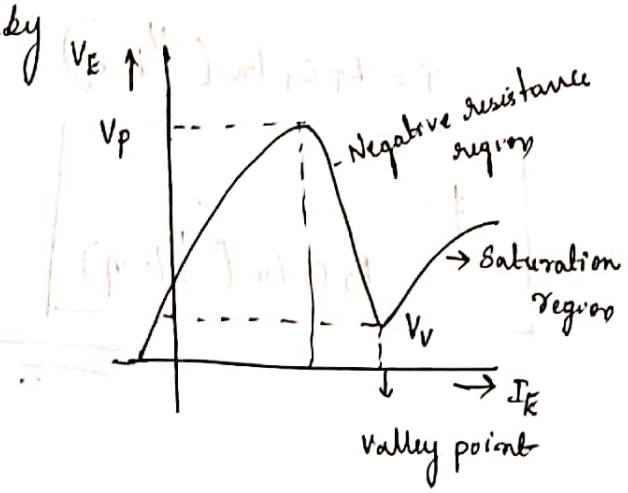
$\eta$ - stand off ratio varies from 0.4 to 0.6

$\eta = 0.5$.

$$f_o = \frac{1}{R_T C_T \ln\left(\frac{1}{1-0.5}\right)}$$

$$f_o = \frac{1.44}{R_T C_T \ln 2} = \frac{1.44}{R_T C_T}$$

$$\boxed{f_o = \frac{1.5}{R_T C_T}}$$



Capacitor $C_T$ is charged through resistor $R_T$ towards supply voltage $V_{BB}$. As long as the capacitor voltage $V_E$ is below a standoff voltage set by the voltage across $B_1 - B_2$ and the transistor standoff ratio $\eta$

As long as the capacitor voltage is less than peak voltage $V_p$ the emitter appears as an open circuit.

$$V_c < V_p$$

$$\boxed{V_p = \eta V_{BB} + V_D}$$

$\eta$ - Standoff ratio of UJT $V_D$ = cut-in voltage of diode.

When the capacitor voltage $V_c$ exceeds the voltage $V_p$ the UJT turns on the capacitor starts discharging through $R_1 + R_{B_1}$, $R_{B_1}$ is assumed as negligible and hence capacitor discharge through $R_1$

$$V_c(t) = V_v + V_{BB}(1 - e^{-t/R_T C_T})$$

$$V_c(t) = V_p \quad \text{at } t = T$$

$$V_p = V_v + V_{BB}(1 - e^{T/R_T C_T})$$

$$\eta V_{BB} + V_B = V_v + V_{BB}(1 - e^{T/R_T C_T})$$

Neglecting $V_D$ and $V_{BB}$ to get the Approximate relation for T.

$$\eta = 1 - e^{-T/R_T C_T}$$

$$T = R_T C_T \ln(1/1-\eta)$$

$$\boxed{f = \frac{1}{R_T C_T \ln(1/1-\eta)}}$$

Assignment questions.

(1) Explain Barkhausen Criterion for oscillation. Also give the classification of oscillators.

(2) Explain how a feedback circuit can be used as oscillator.

(3) Explain the different types of feedback connection types.

(4) Derive the equation for $Z_{if}$, $Z_{of}$ for ① Voltage Series
② Voltage Shunt
③ Current Series
④ Current Shunt.

(5) With neat circuit diagram explain the working of RC phase oscillator using FET and write the equation for frequency of oscillation.

(6) With neat circuit diagram explain the operation of tuned oscillator.

(7) With neat circuit diagram explain the working of tank circuit for tuned oscillator circuit.

(8) With neat circuit diagram explain the working of Crystal oscillators in Series and parallel resonant mode and explain the characteristics of Quartz

(9) Derive the expression for frequency of a wein bridge oscillator and explain the operation using a neat circuit diagram.

(10) Explain the concept of positive feedback used in oscillators?

(11) Explain the practical feedback circuits?

Module-5 Power Amplifiers and Voltage Regulators

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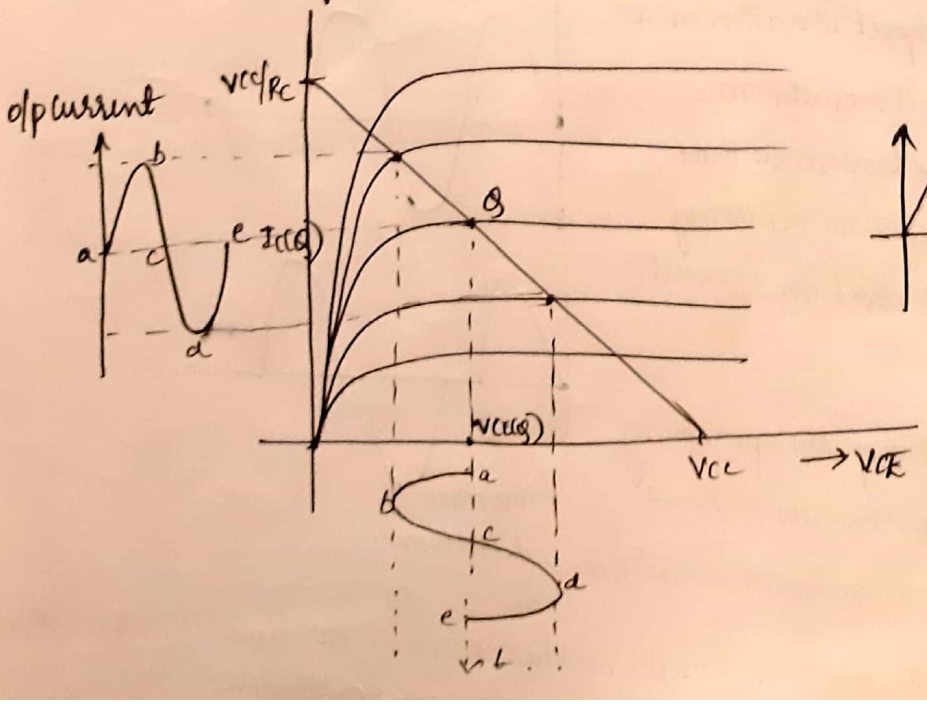
Power Amplifiers are large Signal Amplifiers they increases the power of given input Signal. The power amplifiers converts the dc power of the Supply Voltage to the ac power delivered to the load.

Power Amplifiers are classified based on the location of Q-point and are follows.

1. class A power amplifiers
2. class B power amplifiers
3. class AB power amplifiers
4. class C power amplifiers.

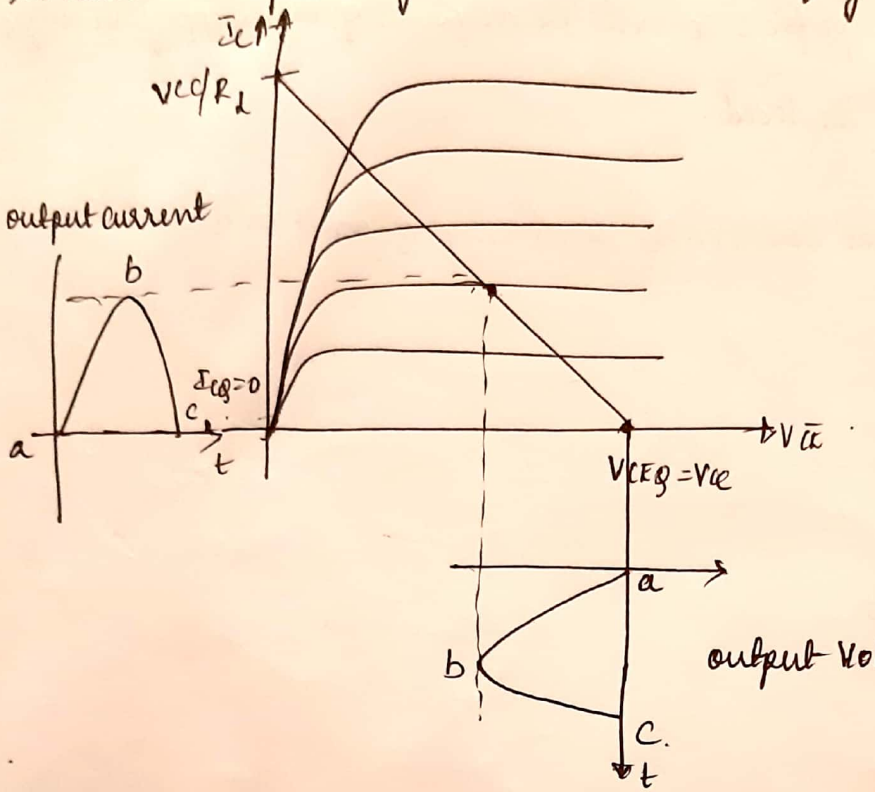
## Class A power amplifier

class A power amplifiers the Q-point is located in Mid point of DC load line So that o/p is obtained for full input cycle i.e for all 360°, Efficiency is small and distortion is very less.



## Class B power amplifiers

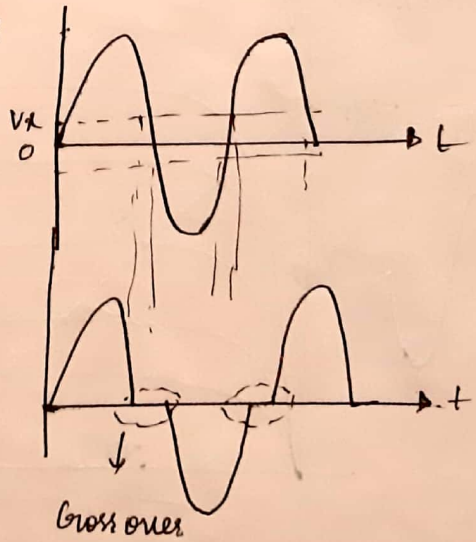
In class B amplifiers the Q-point is located at cut-off so that the so that the output signal varies over one half cycle of the input signal.




Input / output waveforms for a class B power amplifier.

Efficiency of class B amplifiers is much higher than class A amplifier. The harmonic distortion is present due to cut-off Region.

**class AB Amplifier** : The output waveform is not a exact replica of the input waveform. The output signal is distorted observe that the distortion occurs at every zero crossing of the input signal Hence the distortion is called Cross over distortion.



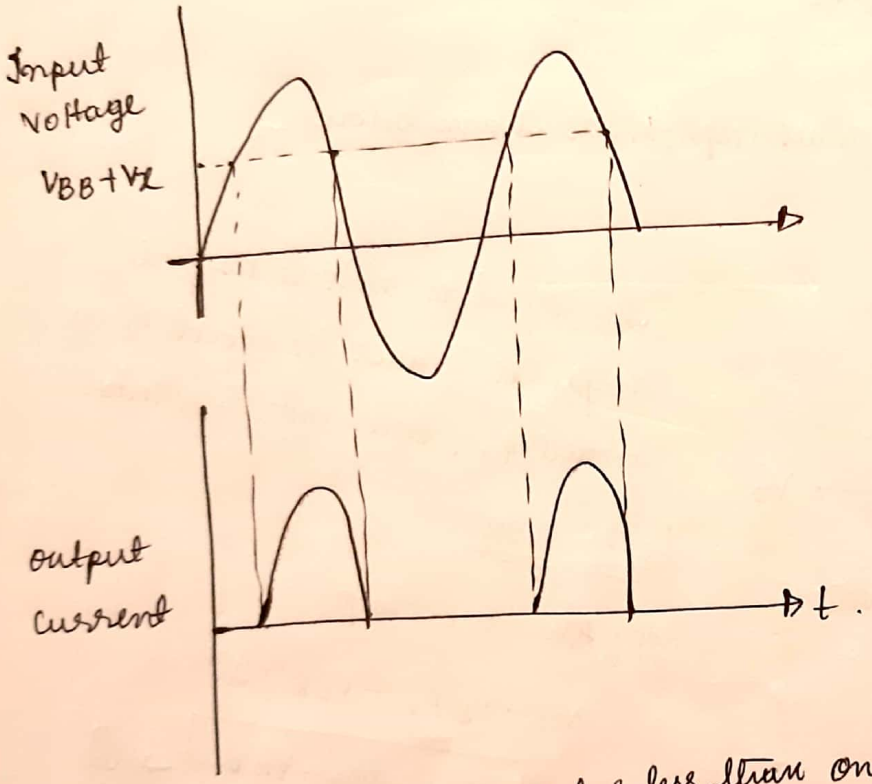

This can be overcome by locating the operating point slightly above cut-off. since the Q-point is located slightly above cutoff as in class B amplifier but much below the centre of the dc load line as in class A amplifier these is referred as class AB power amplifier.

## Class C power Amplifiers

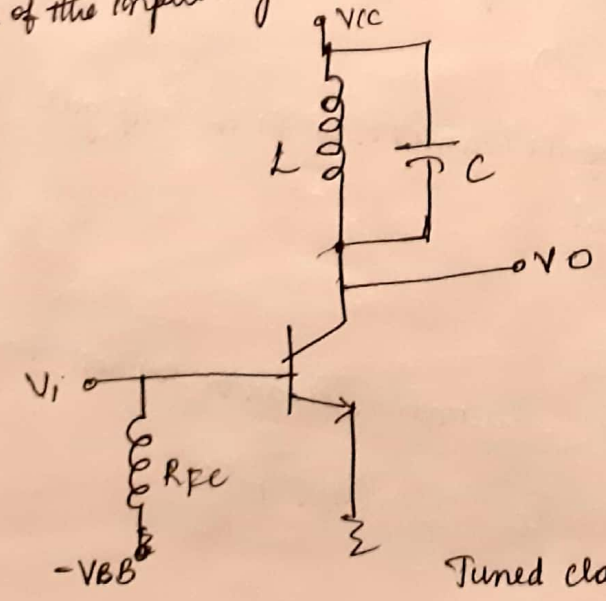
In class C amplifier the transistor is biased below cut-off Let the extent of reverse bias be $V_{BB}$ the transistor operates in the active region and current flows only for $V_i > V_{BB}+V_\gamma$.

$V_\gamma$ = 0.7 Cut in Voltage for Silicon of the base - Emitter junction.

The current would then be pulses of short duration.




The output current flows for less than one half cycle of the input signal the full cycle of the input signal is obtained at the output by the use of a tuned circuit




Tuned class c power amplifier.

## Class A power amplifiers

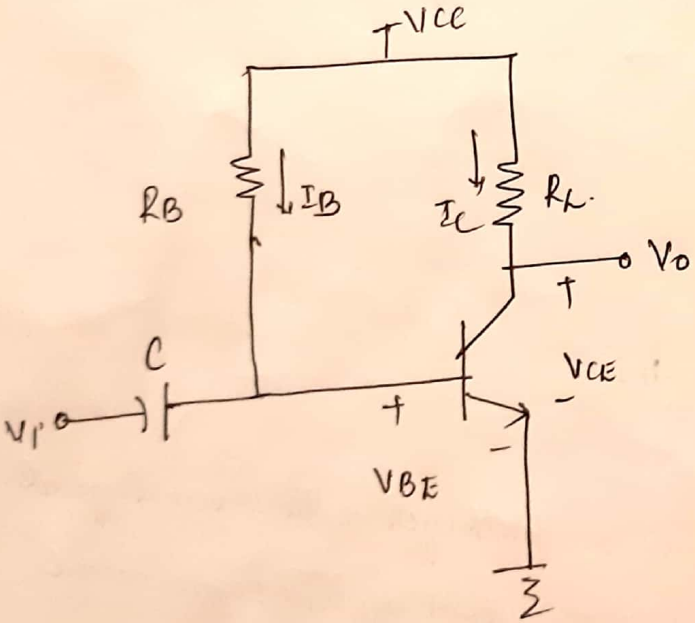
Depending upon how the load is connected at the amplifier output there are two types of class A power amplifiers as given below.

① Series-fed class A power amplifier

② Transformer coupled class A power amplifier.

## Series fed class A power amplifier

A fixed bias series fed class A power amplifier as shown below.




The circuit is called series fed amplifier because the load $R_L$ is connected in series with the collector

### Dc Analysis

Apply KVL to B.E loop

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \rightarrow (1)$$

### Series fed class A large signal amplifier

The collector current $I_C = \beta I_B \rightarrow (2)$

where $\beta$ is the dc current gain of the transistor in the CE configuration.

Apply KVL to the collector to emitter circuit

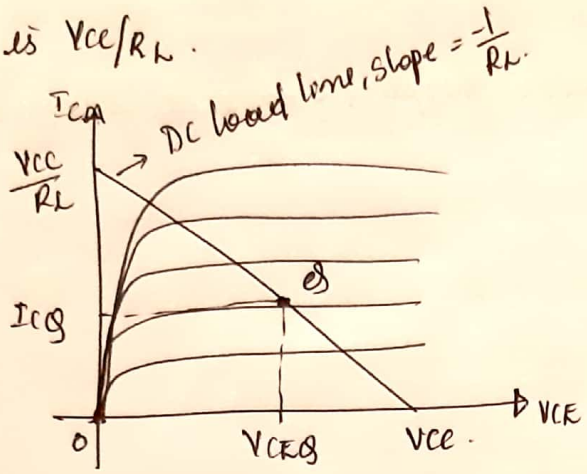
$$V_{CC} = I_C R_L + V_{CE}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_L} \rightarrow (3)$$

Equation (3) can be represented as

$$I_C = -\frac{1}{R_L}(V_{CE}) + \frac{V_{CC}}{R_L}$$

The slope of the dc load line is $\left(-1/R_L\right)$ and the intercept on the current axis is $V_{CC}/R_L$.

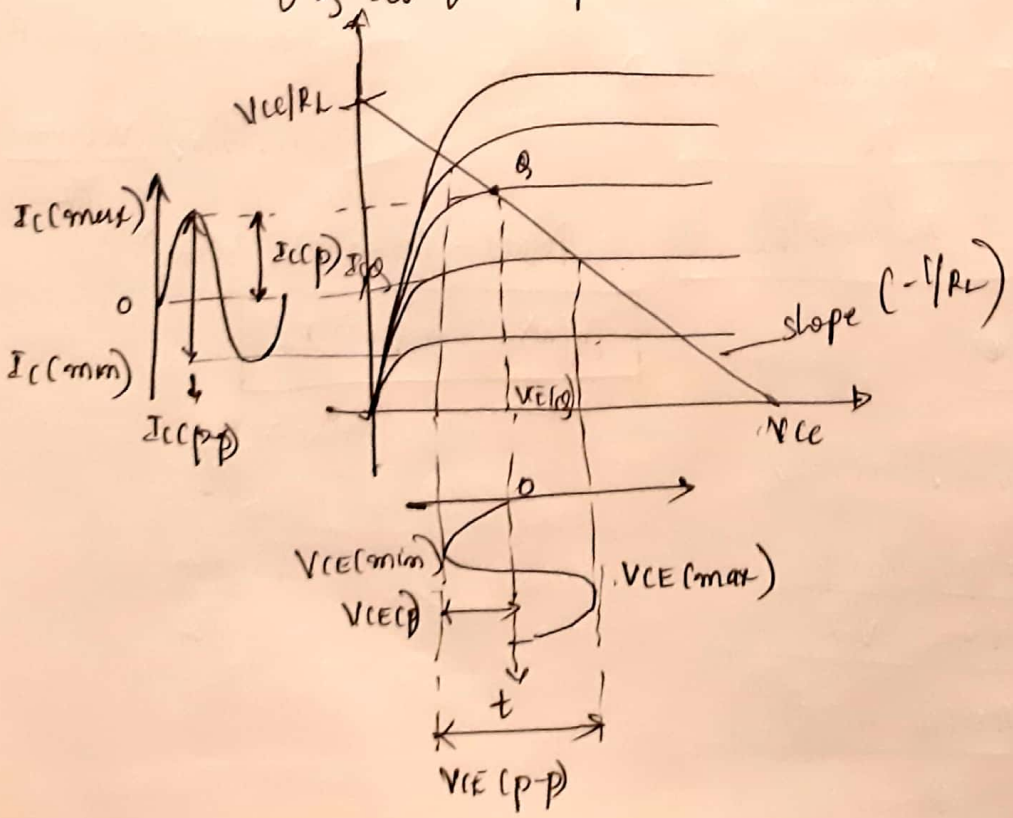



DC load line of class A series fed power amplifier.

## AC analysis

Both the dc current and ac current flows through the same load $R_L$ connected in series with the collector. Hence the ac load line is same as the dc load line. The figure below shows the amplitude of the input signal increases the amplitude of the output current as well as the output voltage increases to a maximum extend bounded by 0 & $V_{CC}/R_L$ for output current

0 & $V_{CC}$ for output voltage



## Power Considerations

For the power amplifiers the input power is supplied from the dc source $V_{CC}$

The dc power i/p is given by

$$P_{i(dc)} = V_{CC} I_{CQ}$$

## Output power (AC power output)

The ac power delivered to the load can be expressed in the following ways.

1. using RMS Values
2. using peak signal values
3. using peak-peak signal values
4. using maximum and minimum values

## using RMS Values

The ac power delivered to the load ($R_L$) is given by.

$$P_{o(ac)} = V_{CE(rms)} \cdot I_{C(rms)} \rightarrow (1)$$

$$= \frac{V_{CE(rms)}}{R_L} \cdot V_{CE(rms)}$$

$$\boxed{P_{o(ac)} = V^2_{CE(rms)} / R_L}$$

By KVL

$$V_{CE(rms)} = I_{CE(rms)} \cdot R_L$$

$$I_{CE(rms)} = \frac{V_{CE(rms)}}{R_L}$$

$$P_{o(ac)} = I_{(rms)} \cdot R_L \, I_{C(rms)}$$

$$\boxed{P_{o(ac)} = I^2_{C(rms)} \cdot R_L}$$

## using peak signal values

$$P_{o(ac)} = V_{CE(rms)} \cdot I_{C(rms)}$$

$$P_{o(ac)} = \frac{V_{CE(p)}}{\sqrt{2}} \frac{I_{C(p)}}{\sqrt{2}}$$

$$\boxed{P_{o(ac)} = \frac{V_{CE(p)} \, I_{C(p)}}{2}}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

## using peak signals

$$P_{o(ac)} = V_{CE(rms)} I_{C(rms)}$$

$$= \frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}}, \quad I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$P_{o(ac)} = \frac{V_{CE(rms)} I_{C(rms)}}{2}$$

$$\boxed{P_{o(ac)} = \frac{V_{CE(p)} I_{C(p)}}{2}}$$

W.K.T

$$V_{CE(p)} = I_{C(p)} \cdot R_L$$

$$I_{C(p)} = \frac{V_{CE(p)}}{R_L}$$

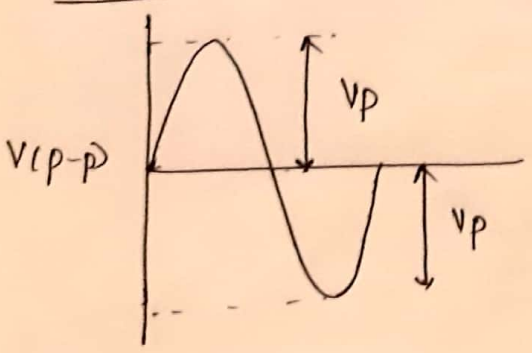
$$P_{o(ac)} = \frac{I_{C(p)} \cdot R_L \cdot I_{C(p)}}{2}$$

$$\boxed{P_{o(ac)} = \frac{I_C^2(p) R_L}{2}}$$

$$P_{o(ac)} = \frac{V_{CE(p)}}{2} \cdot \frac{V_{CE(p)}}{R_L}$$

$$\boxed{P_{o(ac)} = \frac{V_{CE}^2(p)}{2R_L}}$$

## using peak-peak signal




$$V_{(p-p)} = V_p + V_p$$

$$V_{(p-p)} = 2V_p$$

$$V_p = \frac{V_{(p-p)}}{2}$$

$$I_{(p-p)} = I_p + I_p$$

$$I_{(p-p)} = 2I_p$$

$$I_p = \frac{I_{(p-p)}}{2}$$

W.K.T

$$V_{CE(p)} = \frac{V_{CE(p-p)}}{2}$$

$$I_{C(p)} = \frac{I_{C(p-p)}}{2}$$

$$P_{o(ac)} = V_{CE(rms)}\, I_{C(rms)}$$

$$= \frac{V_{CE(p)}}{\sqrt{2}} \frac{I_{C(p)}}{\sqrt{2}}$$

$$= \frac{V_{CE(p-p)}/2 \cdot I_{C(p-p)}/2}{2}$$

$$\boxed{P_{o(ac)} = \frac{V_{CE(p-p)} \cdot I_{C(p-p)}}{8}}$$

Substitute the values in the above equation

W K T

$$I_{C(p-p)} = \frac{V_{CE(p-p)}}{R_L}$$

$$V_{CE(p-p)} = I_{C(p-p)} \cdot R_L.$$

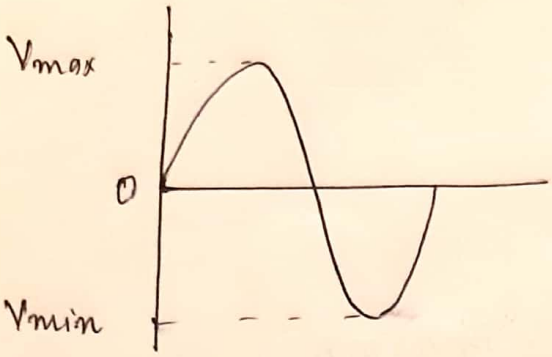
$$P_{o(ac)} = \frac{V_{CE(p-p)}}{8} \cdot \frac{V_{CE(p-p)}}{R_L}$$

$$\boxed{P_{o(ac)} = V_{CE}^2{}_{(p-p)}/8R_L}$$

$$P_{o(ac)} = \frac{I_{C(p-p)} \cdot R_L\, I_{(p-p)}}{8}$$

$$\boxed{P_{o(ac)} = \frac{I_C^2{}_{(p-p)} \cdot R_L}{8}}$$

## using maximum and minimum Values




$$V_{CE(p-p)} = V_{max} - V_{min}$$

$$I_{C(p-p)} = I_{max} - I_{min}$$

$$P_{o(ac)} = \frac{V_{CE(p-p)}\, I_{C(p-p)}}{8}$$

$$P_{o(ac)} = \frac{[V_{max} - V_{min}][I_{max} - I_{min}]}{8}$$

**Efficiency:** The efficiency of an amplifier represents the amount of ac power delivered or transferred to the load from the dc source

$$\% \eta = \frac{P_{o(ac)}}{P_{i(dc)}} \times 100\%$$

**Maximum efficiency:** For maximum swing

$$V_{max} = V_{CC} \text{ \& } V_{min} = 0$$

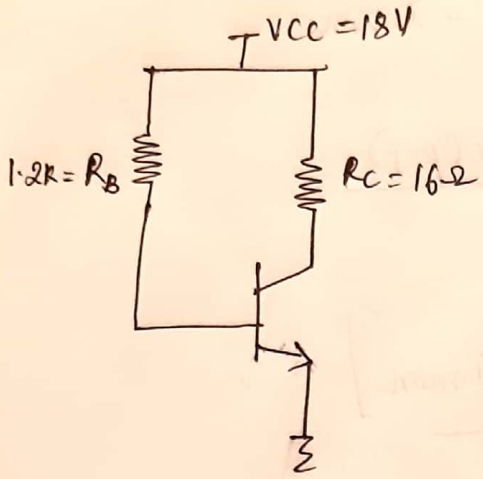
$$I_{max} = 2I_{CQ} \text{ \& } I_{min} = 0$$

$$\text{Maximum } \% \eta = \frac{\text{maximum } P_{o(ac)}}{\text{maximum } P_{i(dc)}} \times 100\%$$

$$= \frac{(V_{max} - V_{min})\,[I_{max} - I_{min}]}{8\, V_{CC} I_{CQ}}$$

$$= \frac{(V_{CC})(2I_{CQ})}{4\, V_{CC} I_{CQ}} \times 100 = 25\%$$

→ Calculate input powers, output powers and efficiency of amplifier shown for an input voltage that results in base current of 5mA (rms). Assume silicon transistor with $\beta = 40$, $V_{BE} = 0.7$




$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B = \frac{18 - 0.7}{1.2K} = 14.42mA$$

$$I_C = \beta I_B = 40 \times 14.42mA = 576.8mA$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = 18 - 576.8mA \times 16\Omega$$

$$\boxed{V_{CE} = 8.77V}$$

$$P_{i(dc)} = V_{CC} I_{CQ}$$

$$= 18 \times 576.8mA$$

$$P_{i(dc)} = 10.4W$$

$$I_{B(rms)} = 5mA$$

$$I_{C(rms)} = \beta \cdot I_{B(rms)}$$

$$= 40 \times 5mA$$

$$\boxed{I_{C(rms)} = 200mA}$$

$$I_{C(rms)} = \frac{I_{C(p)}}{\sqrt{2}}$$

$$I_{C(p)} = \sqrt{2} \cdot I_{C(rms)}$$

$$I_{C(p)} = \sqrt{2} \times 200mA$$

$$\boxed{I_{C(p)} = 282.8mA}$$

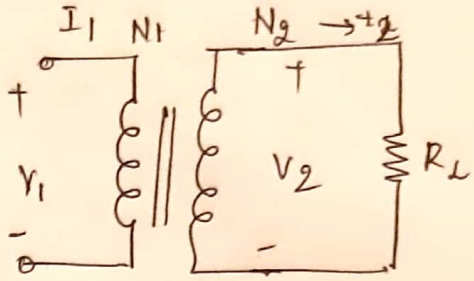
$$P_{o(ac)} = \frac{I_{C(p)}^2 R_L}{2}$$

$$= \frac{(282.8mA)^2}{2} \times 16$$

$$\boxed{P_{o(ac)} = 0.64W}$$

$$\eta = \frac{0.64W}{10.4W} = 6.15\%$$

## Properties of transformer




while analysing the transformer it is assumed that the transformer is ideal if there are no losses in the transformer.

Similarly the winding resistances are assumed to be zero

$N_1$ – No of turns on primary

$N_2$ = No of turns on secondary

$V_1$ = Voltage applied to primary

$V_2$ – secondary voltage

$I_1$ – primary current

$I_2$ – secondary current

**Turns ratio:** The ratio of no of turns on secondary to the no of turns on primary is called turns ratio of the transformer denoted by n

$$\frac{N_2}{N_1} = 1 \quad \text{or} \quad \frac{N_1}{N_2} = 1$$

**Voltage transformation:** The transformer transforms the voltage applied on one side to other side proportional to the turns ratio the transformer can be step up or step down transformer.

$$\frac{V_2}{V_1} = \frac{N_2}{N_1} = n \implies \frac{V_1}{V_2} = \frac{N_1}{N_2}$$

**Current transformation**

$$\frac{I_2}{I_1} = \frac{N_1}{N_2} = \frac{1}{n}$$

Impedance transformation: load on the Secondary

$$R_L = \frac{V_2}{I_2} \qquad R_L' = \frac{V_1}{I_1}$$

where $R_L'$ is the load reflected at the primary

$$\frac{V_1 I_2}{V_2 I_1} = \frac{N_1^2}{N_2^2}$$

$$\frac{(V_1/I_1)}{(V_2/I_2)} = \left(\frac{N_1}{N_2}\right)^2$$

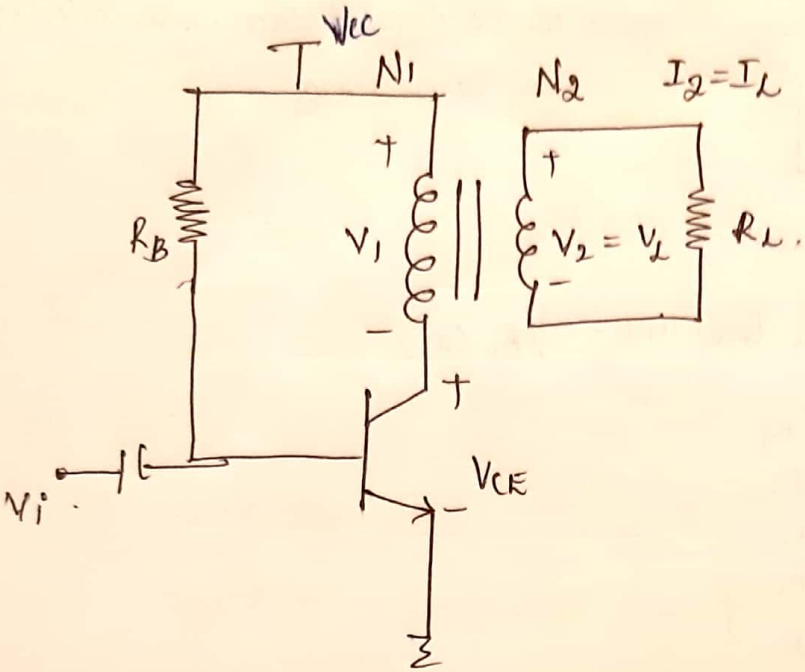
$$\frac{R_L'}{R_L} = \left(\frac{N_1}{N_2}\right)^2$$

$$R_L' = R_L \left(N_1/N_2\right)^2$$

$$\boxed{R_L' = \frac{R_L}{n^2}}$$

$R_L' > R_L$ can be achieved by choosing $N_1 > N_2$ i.e we have to use a step down transformer of appropriate turns ratio.

# Transformer Coupled class A power Amplifier




## DC operations

→ It is assumed that the winding resistances are zero

→ There is no dc voltage drop across primary of transformer the slope of the dc load line is reciprocal of the dc resistance in the collector circuit

$$1/R_{(dc)} = 1/0 = \infty.$$

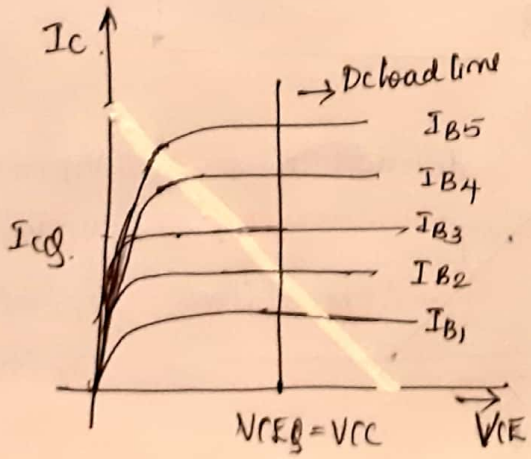
Apply KVL to the collector circuit

$$V_{CC} = V_{CE} = 0$$

$$\boxed{V_{CEQ} = V_{CC}}$$

This is the dc bias voltage $V_{CEQ}$ for the transistor.

Hence the dc load line is a vertical straight line passing through a voltage point on the x-axis which is $V_{CEQ} = V_{CC}$



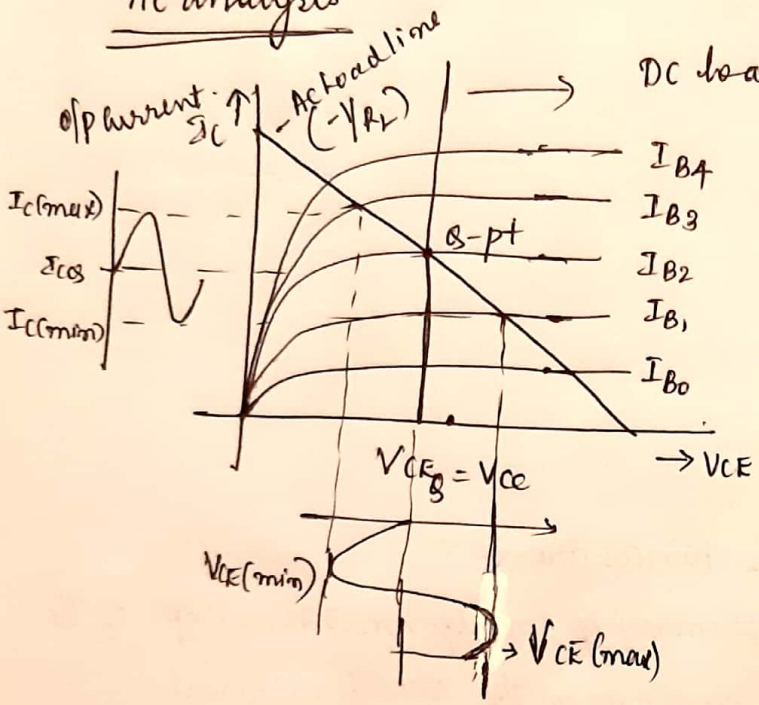

Slope = $-1/R_{L(dc)}$

## DC input power

The dc i/p power is given as the dc current drawn is collector bias current $I_{CQ}$

$$P_{i(dc)} = V_{CC} I_{CQ}$$

## AC analysis




→ The load resistance $R_L$ is connected across the secondary of the transformer

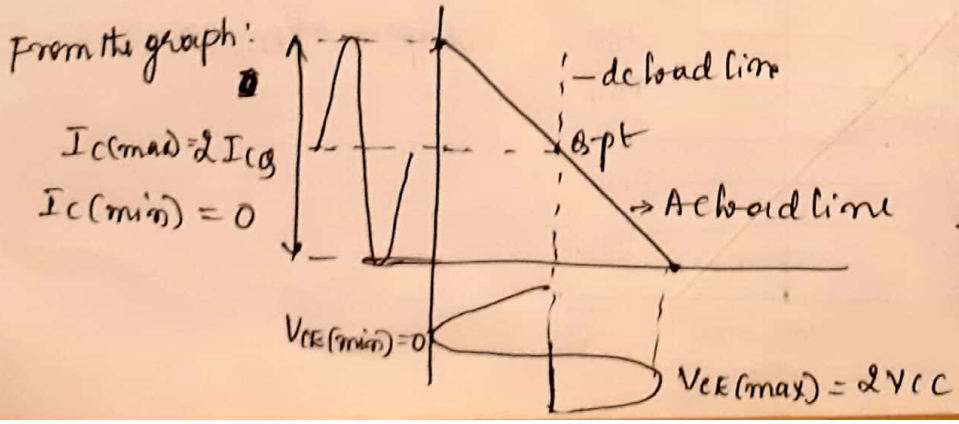
→ The reflected load resistance $R_L'$ is calculated using the formula.

$$R_L' = \left(\frac{N_1}{N_2}\right)^2 R_L$$

Expression for AC output power: WKT $P_{o(ac)}$ from Series fed class A power amplifier

$$P_{o(ac)} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}$$

From the graph:




$V_{CE(max)} = 2V_{CC}$

$V_{CE(min)} = 0$

$I_{C(max)} = 2I_{CQ}$

$I_{C(min)} = 0$

$$P_{ac} = \frac{(2V_{cc} - 0)(2I_{CQ} - 0)}{8}$$

$$= \frac{4 V_{cc} I_{CQ}}{8}$$

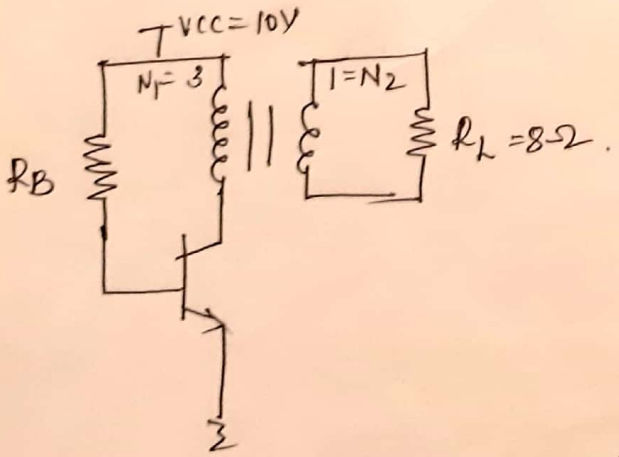
$$\boxed{P_{o(ac)} = \frac{V_{cc} I_{CQ}}{2}}$$

Efficiency $\eta = \frac{P_{o(ac)}}{P_{i(dc)}} \times 100$

$$= \frac{\frac{V_{cc} I_{CQ}}{2}}{V_{cc} I_{CQ}} \times 100$$

$$\boxed{\eta = 50\%}$$

→ For the transformer coupled class A power amplifier the dc base current is 5mA and ac input signal result in a peak base current swing of 4mA. Assume the silicon transistor with $\beta = 30$ find $P_{i(dc)}$, $P_{o(ac)}$ & $\eta$.




$I_B = 5mA$

$I_{B(p)} = 4mA$ $\quad \frac{N_1}{N_2} = 3$

$\beta = 30$

$V_{CC} = 10V$

$V_{CE(Q)} = V_{CC} = 10V$

$I_{CQ} = \beta I_B = 30 \times 5 = 150mA$

$I_{C(p)} = \beta \cdot I_{B(p)} = 30 \times 4mA = 120mA$

$P_{i(dc)} = V_{CC} I_{CQ} = 10 \times 150mA = 1.5W$

$P_{o(ac)} = \frac{I_{C(p)}^2}{2} R_L' = \frac{(120)^2}{2} \times 72\Omega = 0.52W$

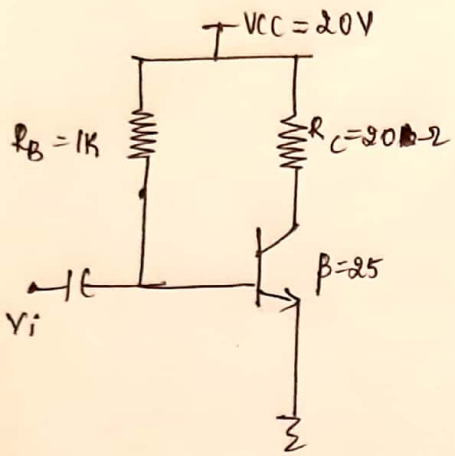
$R_L' = R_L (N_1/N_2)^2$

$= 8\Omega \times 9$

$= 72\Omega$

$\boxed{\eta = \frac{0.52W}{1.5W} = 34.7\%}$

Calculate the i/p power and o/p power and $\eta$ of amplifier circuit as shown below. for an input voltage that results in a base current of 10mA peak.




$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20 - 0.7}{1K} = 19.3mA$$

$$I_{CQ} = \beta I_B = 25 \times 19.3mA = 0.48A$$

$$V_{CE} = V_{CC} - I_C R_C = 20V - (0.48 \times 20\Omega) = 10.4V$$

$$I_{C(p)} = \beta \cdot I_{B(p)} = 25 \times 10mA = 250mA$$

$$P_{i(dc)} = V_{CC} I_{CQ} = 20 \times 0.48 = 9.6W$$

$$P_{o(ac)} = \frac{I_{C(p)}^2}{2} R_L = \frac{(250mA)^2}{2} \times 20K = 0.625W.$$

$$\eta = \frac{P_{o(ac)}}{P_{i(ac)}} = \frac{0.625}{9.6W} = 6.5\%.$$

## Conversion efficiency for class A power Amplifiers

The amplifiers convert the dc power of the supply $V_{cc}$ into ac signal power at the load. The ratio of the ac power delivered to the load to the dc power supplied to the power amplifier is called the conversion efficiency

$$\%\eta = \frac{\text{ac or signal power delivered to the load.}}{\text{dc power supplied to the amplifier.}} \times 100\%$$

$$\%\eta = \frac{P_{o(ac)}}{P_{i(dc)}} \times 100\% \quad \rightarrow (1)$$

$$P_{o(ac)} = \frac{V_{CE(p)}\, I_{C(p)}}{2} \quad \rightarrow (2)$$

$$P_{i(dc)} = V_{CC} I_{CQ} \quad \rightarrow (3)$$

Substituting in Equation (1) we get.

$$\%\eta = \frac{V_{CE(p)}\, I_{C(p)}}{2 \cdot V_{CC} \cdot I_{CQ}}$$

$$\boxed{\%\eta = 50\left[\frac{V_{CE(p)}\, I_{C(p)}}{V_{CC} \cdot I_{CQ}}\right]} \quad \rightarrow (4)$$

## Conversion efficiency of class A series fed power Amplifier.

$$V_{CE(p)} = \frac{V_{CE(max)} - V_{CE(min)}}{2}$$

Substituting this value in the equation (4) we get.

$$\%\eta = \frac{50\left[V_{CE(max)} - V_{CE(min)}\right] I_{C(p)}}{2 V_{CC} I_{CQ}}$$

$$= \frac{25\left[V_{CE(max)} - V_{CE(min)}\right] I_{C(p)}}{V_{CC} \cdot I_{CQ}}$$

$$I_{CQ} = I_{C(p)}$$

$$\boxed{\%\eta = \frac{25\left[V_{CE(max)} - V_{CE(min)}\right]}{V_{CC}}}$$

If $V_{CE(max)} = V_{CE}$

$V_{CE(min)} = 0$

$\eta = 25\%$

Conversion efficiency for transformer coupled class A power amplifier.

$$V_{CC} = \frac{V_{max} + V_{min}}{2} \qquad V_{CE(p)} = \frac{V_{CE(max)} - V_{CE(min)}}{2}$$

$I_{CQ} = I_{C(p)}$

$$\%\eta = \frac{50\, V_{CE(p)}\, I_{C(p)}}{V_{CC} \cdot I_{CQ}}$$

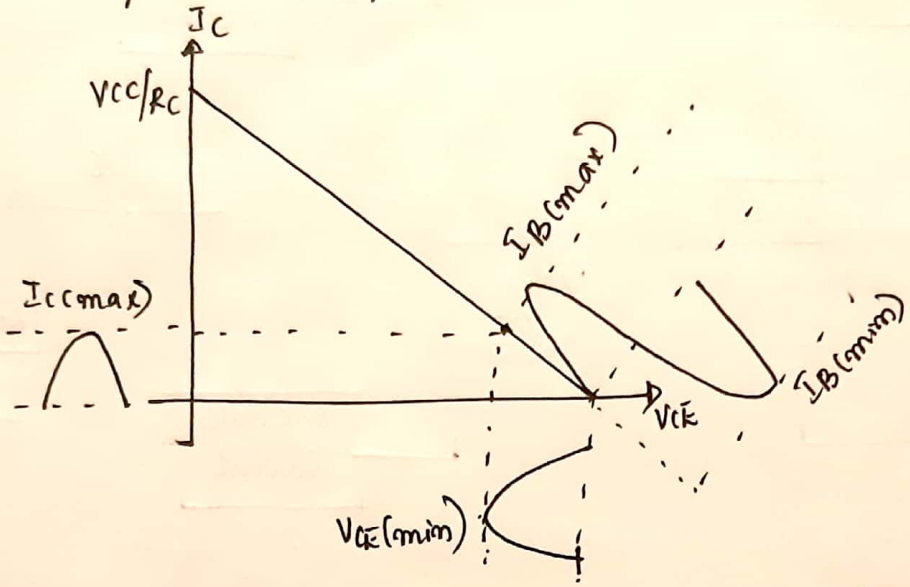
$$= 50\left[\frac{\frac{V_{CE(max)} - V_{CE(min)}}{2}}{\frac{V_{CE(max)} + V_{CE(min)}}{2}}\right]$$

$$\boxed{\eta = 50\%\left[\frac{V_{CE(max)} - V_{CE(min)}}{V_{CE(max)} + V_{CE(min)}}\right]}$$

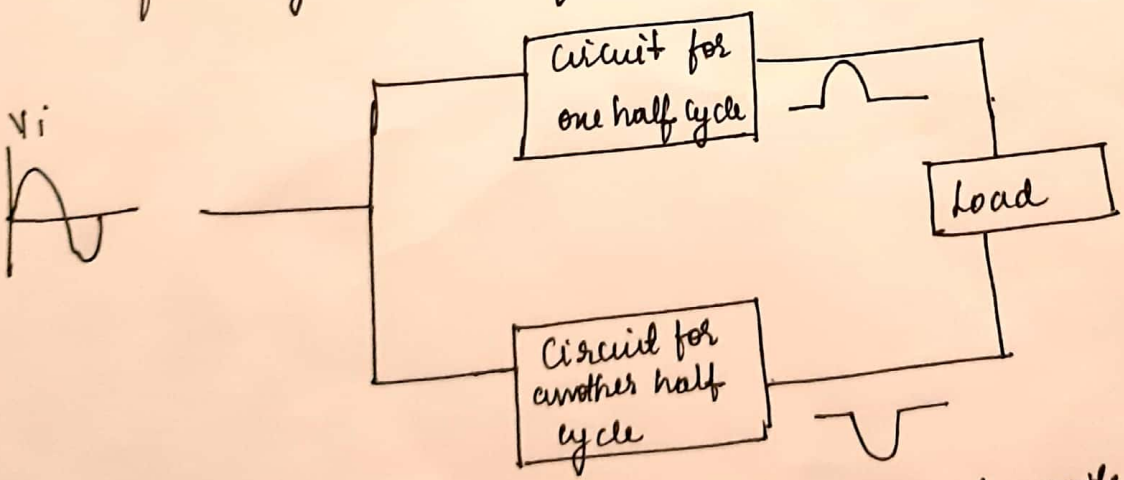
$V_{CE(min)} \to 0$

$$\boxed{\eta = 50\%}$$

In class B operation Q point lies exactly on the x-axis. in this location transistor operates for only one half cycle and in remaining half cycle its off

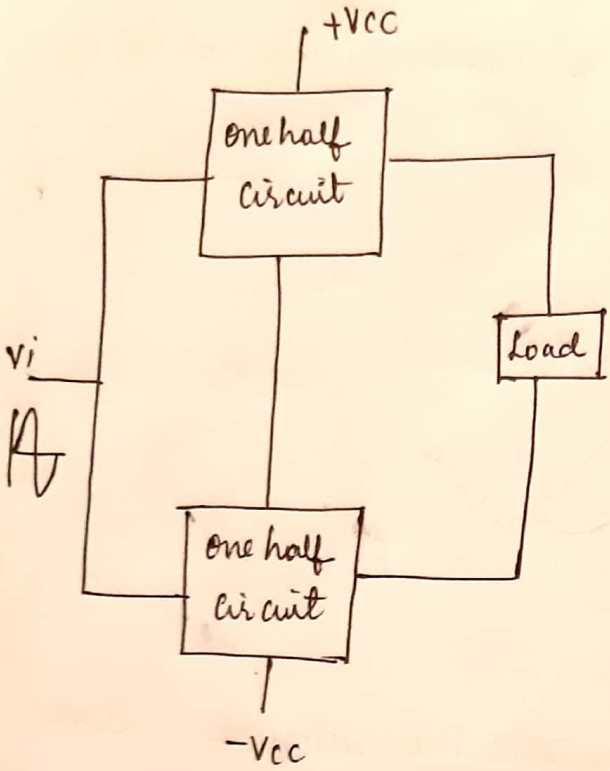


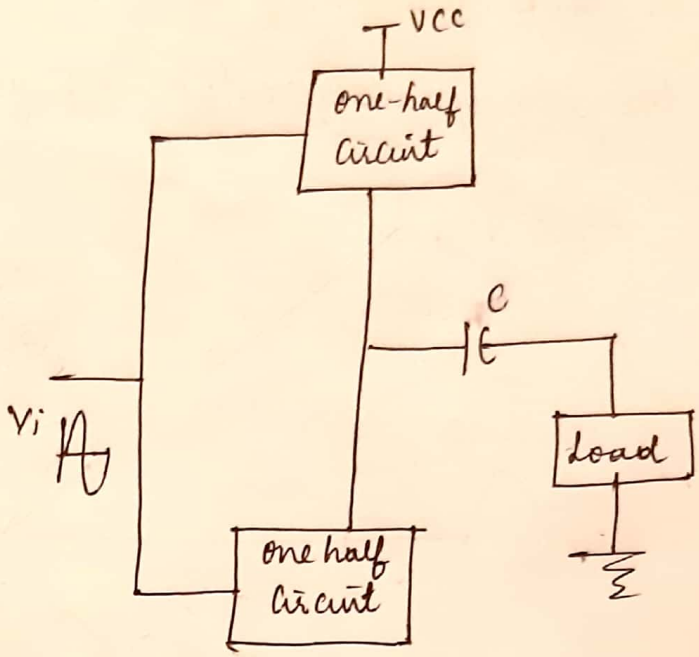

To obtain full half cycle it is necessary to use two transistors such that one is ON for positive half cycle and other is ON for negative half cycle Therefore the general block diagram for class B power amplifier can be written as




Since the above circuit tries to push the signal upside (towards +Ve side) and the below circuit tries to pull the signal downside towards negative side class B Amplifier is also called as push-pull Amplifier

Block diagram of push-pull amplifier using single voltage and two voltage supplies.




Class B power-Amplifier using single source and two sources.

## Expression for AC output power.

The ac output power $P_{o(ac)} = \frac{V_{CE(p)} I_{C(p)}}{2}$

$$I_{C(p)} = \frac{V_{CE(p)}}{R_L}$$

$$\boxed{P_{o(ac)} = \frac{V_{CE}^2(p)}{2R_L}}$$

The ac output power is maximum when $V_{CE(p)} = V_{CC}$

$$\boxed{P_{o(ac)} = \frac{V_{CC}^2}{2R_L}} \quad \therefore I_{C(p)} = \frac{V_{CC}}{R_L}.$$

The dc output power:

$$P_{i(dc)} = V_{CC} \cdot I_{CQ}$$
$$= V_{CC} \cdot I_{dc}$$

$$I_{CQ} = I_{dc} = \frac{2I_m}{\pi}$$

$$P_{i(dc)} = V_{CC} \cdot \frac{2 \cdot I_{C(p)}}{\pi}$$

$$I_{CQ} = I_{dc} = \frac{2 \cdot I_{C(p)}}{\pi}$$

$$P_{i(dc)} = \frac{V_{CC} \cdot 2 \cdot V_{CC}}{\pi \cdot R_L}$$

$$\boxed{P_{i(dc)} = \frac{2V_{CC}^2}{\pi R_L}}$$

Efficiency: $\eta = \frac{P_{o(ac)}}{P_{i(dc)}}$

$$\eta = \frac{\frac{V_{CC}^2}{2R_L}}{\frac{2V_{CC}^2}{\pi R_L}}$$

$$= \frac{V_{cc}^2}{2R_L} \times \frac{\pi R_L}{2V_{cc}^2}$$

$$\eta = \pi/4$$

$$\eta = 0.784 \times 100$$

$$\boxed{\eta = 78.4\%}$$

Efficiency in terms of peak load current & peak load voltage

$$P_{o(ac)} = \frac{V_{CE(p)} I_{C(p)}}{2}$$

$$P_{o(ac)} = \frac{V_{L(p)} \cdot I_{L(p)}}{2}$$

$$I_{C(p)} = I_{L(p)} = \frac{V_{L(p)}}{R_L}$$

$$\boxed{P_{o(ac)} = \frac{V_L^2(p)}{2R_L}}$$

$$P_{i(dc)} = V_{cc} \cdot I_{CQ}$$

$$\boxed{P_{i(dc)} = V_{cc} \cdot \frac{2}{\pi} I_{L(p)}}$$

$$I_{L(p)} = \frac{V_{L(p)}}{R_L}$$

$$\eta = \frac{P_{o(ac)}}{P_{i(dc)}} = \frac{\frac{V_L^2(p)}{2R_L}}{V_{cc} \cdot \frac{2}{\pi} \frac{V_{L(p)}}{R_L}}$$

$$V_{L(p)} = V_{cc}$$

$$= \frac{\frac{V_{cc}^2}{2R_L}}{\frac{2V_{cc}^2}{\pi R_L}} = \pi/4 = 0.784 \times 100$$

$$\boxed{\eta = 78.4\%}$$

Power dissipated by output transistos : The power dissipates in transistors as heat and is given by

$P_{2Q} = P_{i(dc)} - P_{o(ac)}$ ⇒ for two transistors

$P_Q = \frac{P_{2Q}}{2}$ ⇒ for one transistor

(2) Derive an expression for maximum input power and output power

$P_{i(dc)} = V_{cc} \cdot I_{dc}$

$= V_{cc} \cdot \left(\frac{2 I_{max}}{\pi}\right)$

$= V_{cc} \cdot \left(\frac{2 \cdot V_{L(max)}}{\pi R_L}\right)$

$I_{max} = \frac{2 V_{L(max)}}{\pi R_L}$

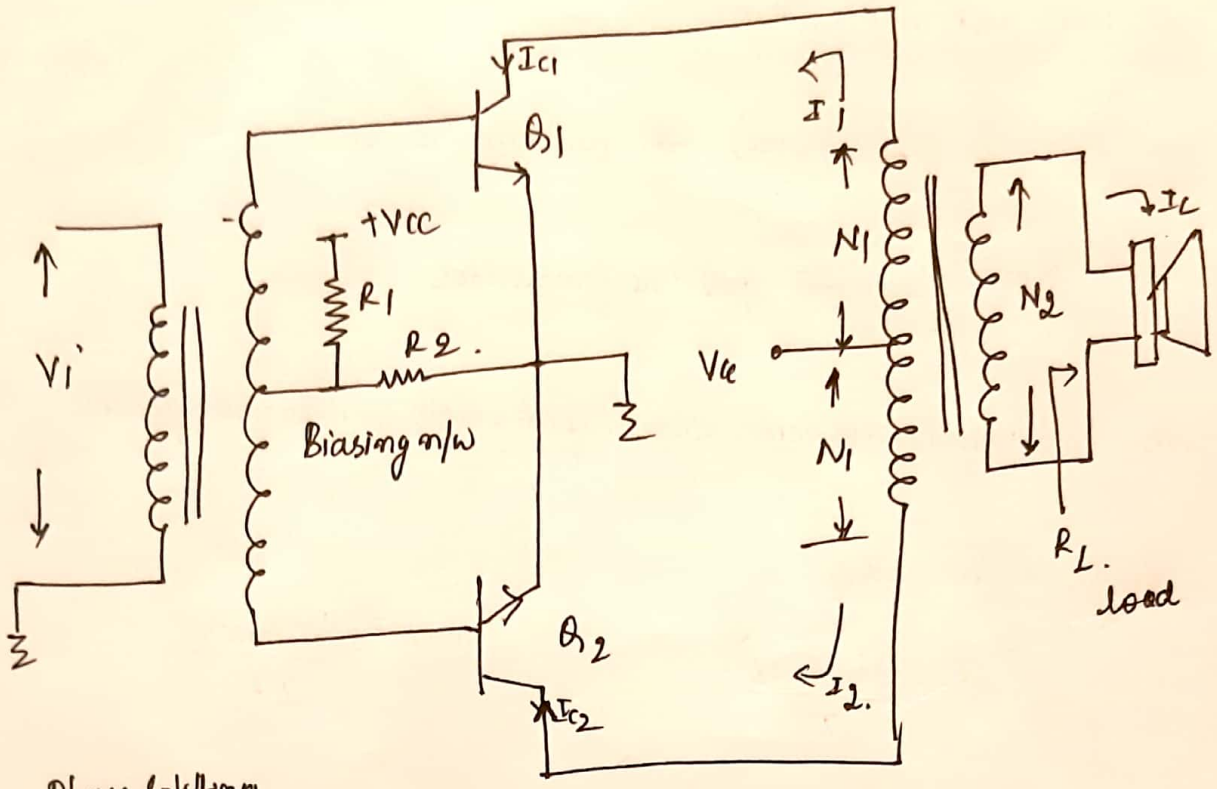
$V_{L(max)} = V_{cc}$

$$\boxed{P_{i(dc)max} = \frac{2 V_{cc}^2}{\pi R_L}}$$

$P_{o(ac)} = \frac{V_{Lmax}^2}{2 R_L}$ But maximum values of $V_{L(max)} = V_{cc}$

$$\boxed{P_{o(ac)} = \frac{V_{cc}^2}{2 R_L}}$$

# Transformer coupled class B push pull circuit




Phase splitting input transformer

Push pull circuit connection

push pull o/p transformer.

The circuit above shown uses a centre tapped input transformer to produce opposite polarity signals to the two transistor inputs and an output transformer to drive the load in a push pull mode.

During the first half cycle of operation transistor $Q_1$ is driven into conduction whereas transistor $Q_2$ is driven off. The current $I_1$ through the transformer results on the first half cycle of signal to the load.

During the second half cycle of the input signal $Q_2$ conducts whereas $Q_1$ stays off the current $I_2$ through the transformer resulting in the second half cycle of the load the overall signal developed across the load then varies over the full cycle of

Signal operation.

During positive half cycle thus $i_{c_1}$ increases above zero ($i_{c_2}=0$) then load current across $Q_1$

$$i_L = \frac{N_1}{N_2} i_{c_1}$$

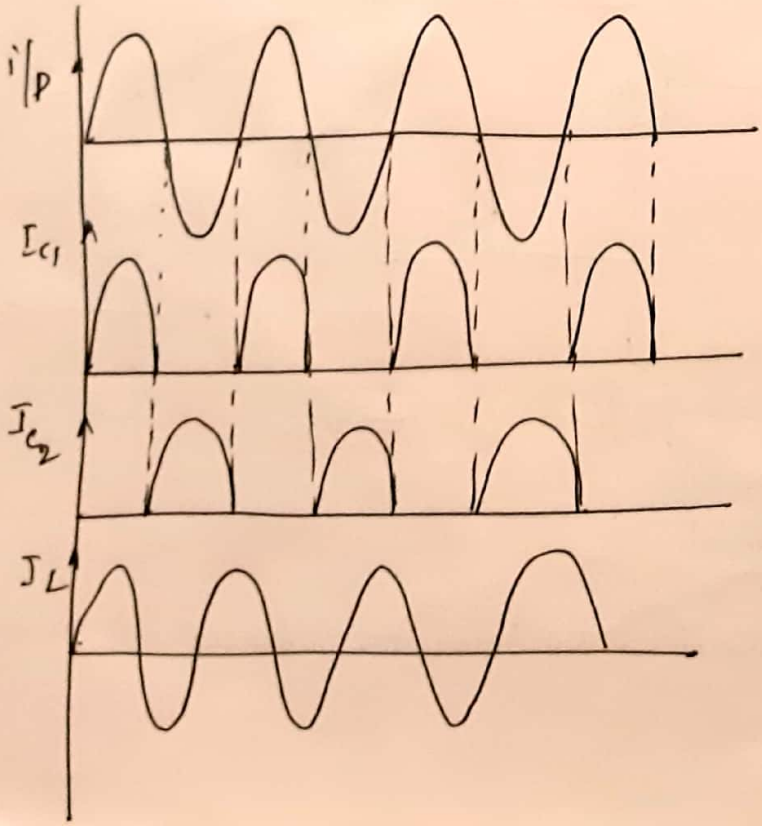
During negative half cycle thus $i_{c_2}$ will be increasing above zero ($i_{c_1}=0$) then load current across $Q_2$

$$i_L = -\frac{N_1}{N_2} i_{c_2}$$

The negative sign for $i_L$ is due to the fact that $i_{c_1}$ and $i_{c_2}$ are in opposite direction

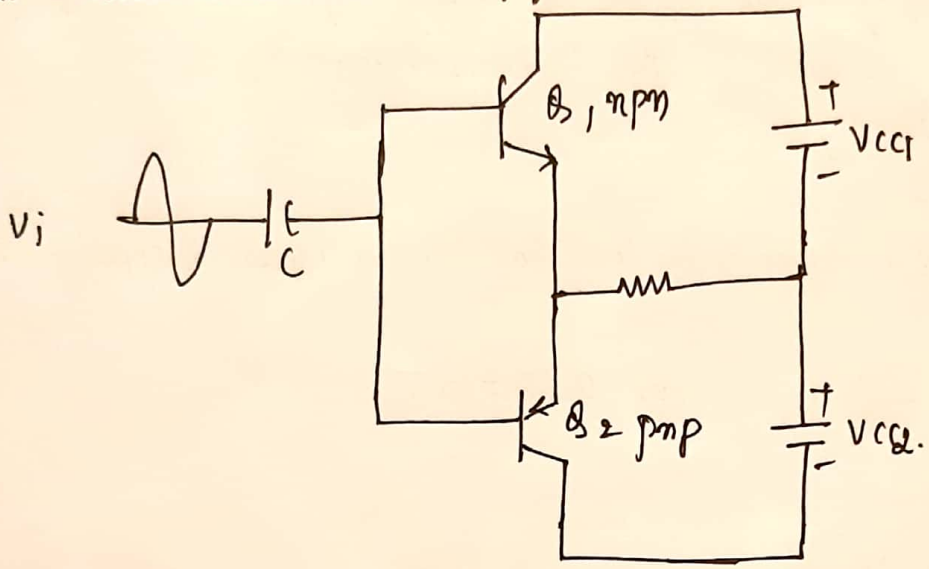
$$i_L = \begin{cases} \frac{N_1}{N_2} i_{c_1} & \text{for } 0 \le \omega t \le \pi \\ -\frac{N_1}{N_2} i_{c_2} & \text{for } \pi \le \omega t \le 2\pi. \end{cases}$$

$$\boxed{i_L = \frac{N_1}{N_2}\left(i_{c_1} - i_{c_2}\right)}$$

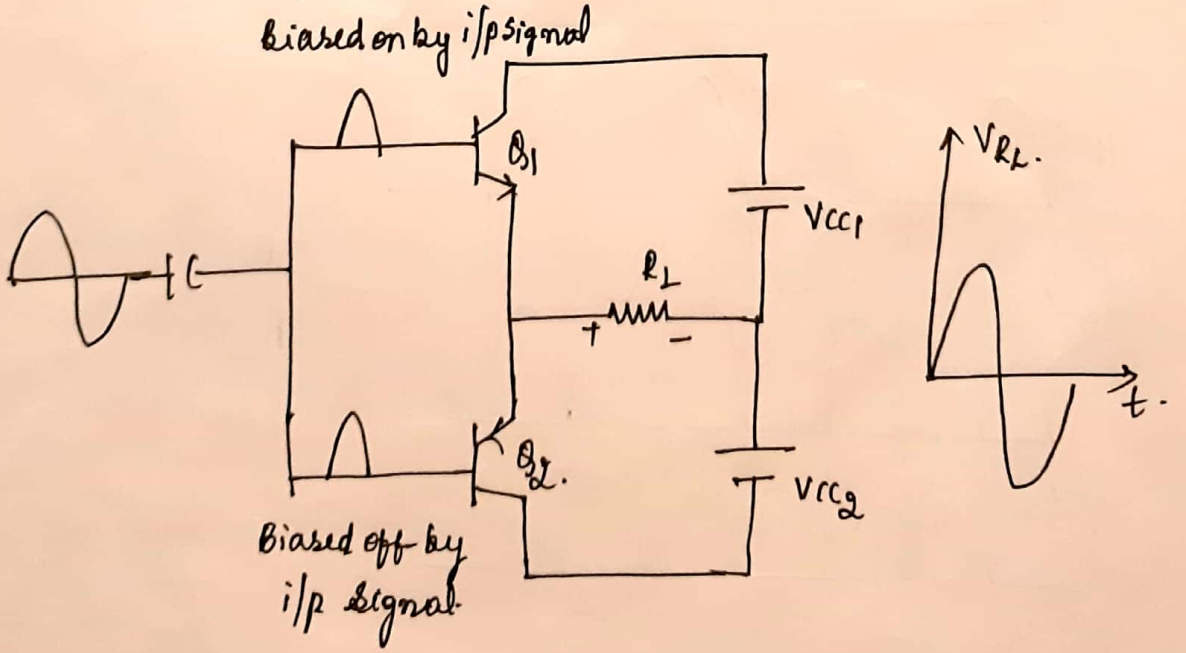


## Complementary-symmetry circuits

using complementary transistors (npn & pnp) it is possible to obtain a full cycle output across a load using half cycles of operation from each transistor as shown in figure below.

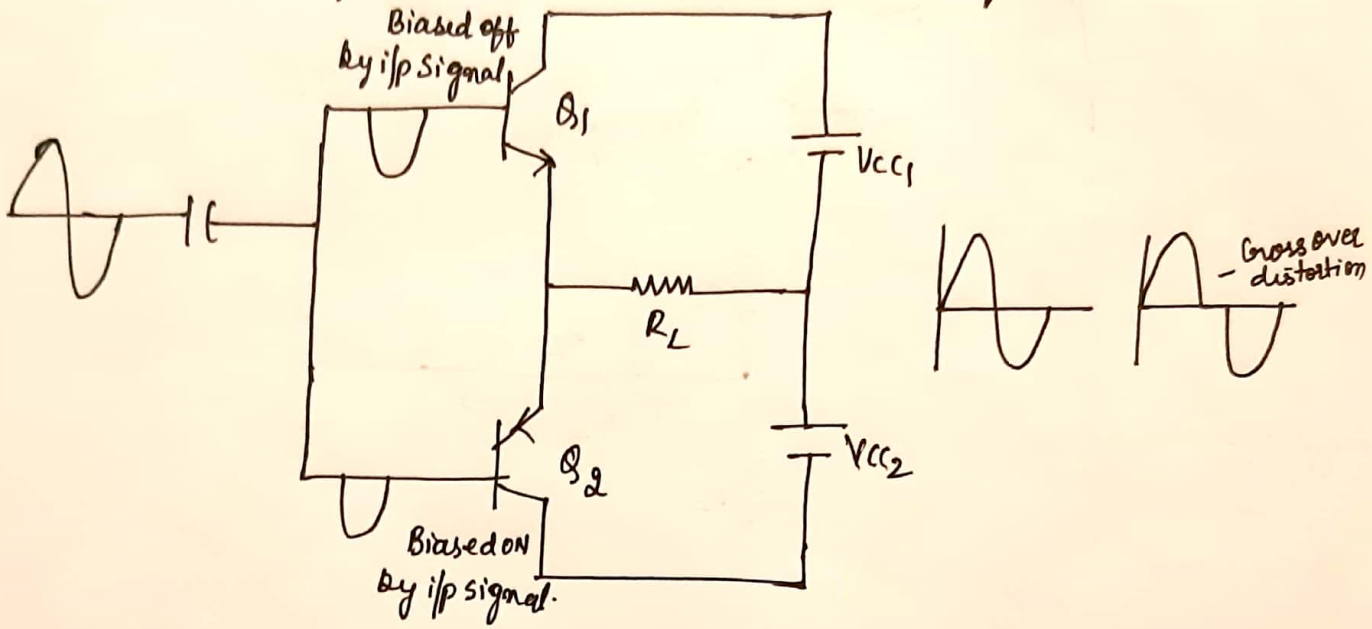



while a single input signal is applied to the base of both transistors the transistors being of opposite type will conduct on opposite half cycles of the input. The npn transistor will be biased into conduction by the positive half cycle of signal with a resulting half cycle of signal across the load.




During negative half cycle of signal the pnp transistor is biased into conduction when the input goes negative.

During a Complete cycle of the input a Complete cycle of output signal is developed across the load. one disadvantage of the circuit is the need for two seperate voltage supplies. Another less obvious disadvantage with the Complementary circuit is shown in the resulting Crossover distortion in the output signal

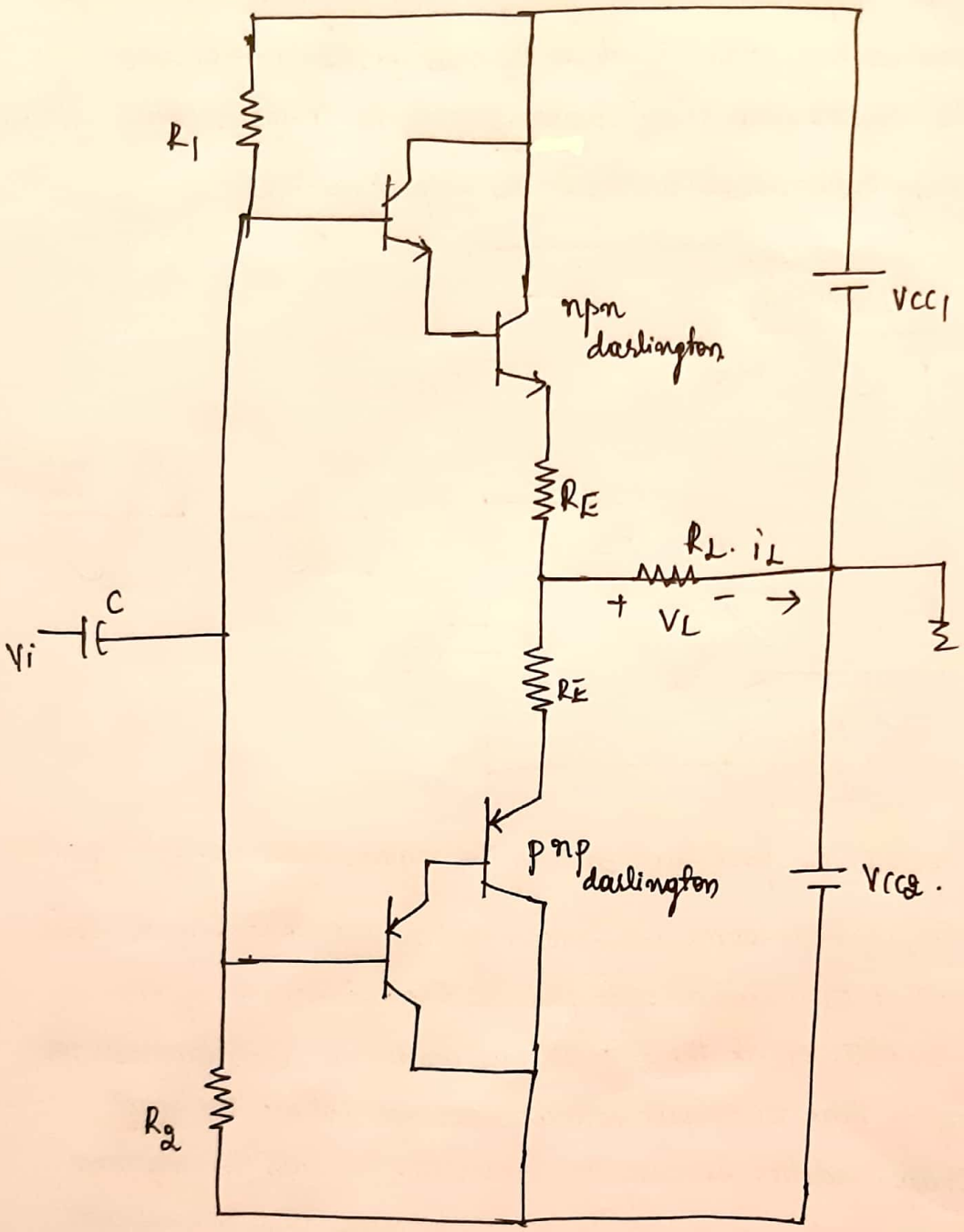



Cross over distortion refers to the fact that during the signal cross overs from positive to negative (or viceversa) there is some non-linearity in the output signal. This results from the fact that the circuit does not provide exact switching of one transistor off and the other on at the zero voltage condition. Both transistors may be partially off so that the output voltage does not follow the input around the zero voltage condition biasing the transistors in class AB improves this operation by biasing both transistors to be on for more than a half cycle.

## Complementary symmetry push pull circuit using darlington transistors

A more practical version of a push pull circuit using complementary transistors is shown in figure. The circuit uses complementary darlington connected transistors to provide higher o/p current and lower output resistance

The circuit provides higher output current and lower output resistance Here the load resistance is matched by low output resistance of the driving source




The biasing resistors $R_1$ and $R_2$ keep the darlington transistors in the verge of conduction as a result the cross over distortion is absent

The low output impedance of the darlington transistor properly match the low impedance of the load which is usually a loud speaker

The darlington transistor provide higher output current

A small amount of negative feedback provided through the emitter resistor $R_E$ helps to keep the harmonic distortion at a minimum.

## Amplifier distortion

→ Any signal varying over less than the full 360° cycle is considered to have distortion.

→ Any ideal amplifier is capable of amplifying a pure sinusoidal signal to provide a larger version the resulting waveform being a pure sinusoidal frequency sinusoidal signal.

→ when distortion occurs output will not be exact duplicate of input signal

→ Distortion can occur because the device characteristic is not linear in this case non linear or amplitude distortion occurs

→ Distortion can also because the circuits elements and devices respond to the input signal differently at various frequencies this being frequency distortion

→ one technique for describing distorted but period waveforms uses fourier analysis a method that describes any periodic waveform in terms of its fundamental frequency component and frequency components at integer multiples these components are called harmonic components or harmonics.

## Harmonic distortion

A signal is considered to have harmonic distortion when there are harmonic frequency components

If the fundamental frequency has amplitude $A_1$ and nth frequency component has an amplitude of $A_n$

Harmonic distortion can be defined as

% $n^{th}$ harmonic distortion $= \% D = \frac{|A_n|}{|A_1|} \times 100\%$.

## Total harmonic distortion

When an output signal has a number of individual harmonic distortion components the signal can be seen to have a total harmonic distortion based on the individual elements as combined by relation.

$$THD = \sqrt{D_2^2 + D_3^2 + D_4^2 + \cdots} \times 100 .$$

## Second harmonic distortion

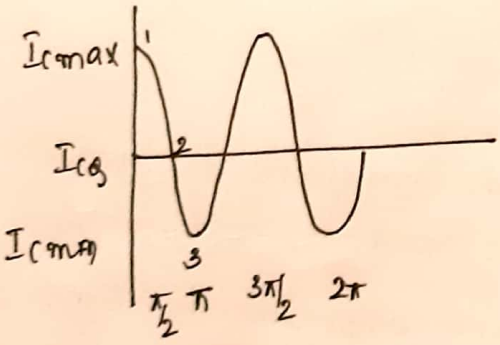



Figure shows a waveform to use for obtaining second harmonic distortion.

A collector current waveform is shown with the quiescent, minimum, maximum signal levels.

An equation that approximately describes the distorted signal waveform is

$$I_c = I_{cQ} + I_0 + I_1 \cos \omega t + I_2 \cos 2\omega t + I_3 \cos 3\omega t + \cdots$$

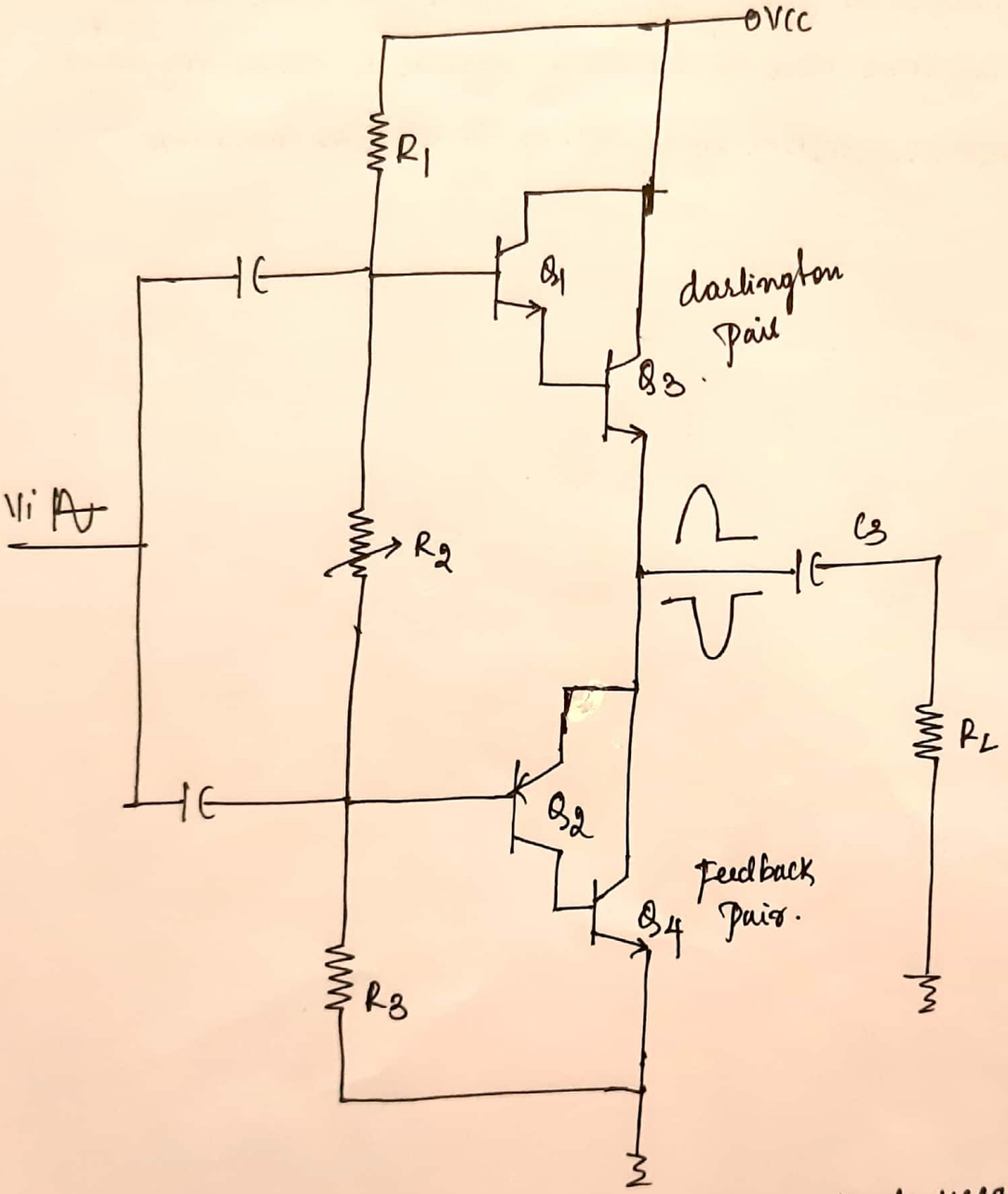
where $I_{cQ}$ = Quiescent current

$I_0$ - additional dc current due to non zero average of the distorted signal

$I_1$ - fundamental component of current

$I_2$ - second harmonic current due to twice the fundamental frequency.

# Quasi complementary class B push pull power Amplifier




In practical power amplifiers circuits it is preferable to use a pnp high power transistor. A practical means of obtaining complementary operation while using the same matched npn transistors for the output is provided by a quasi complementary circuit

The push pull operation is achieved by using complementary transistors $Q_1$ & $Q_2$ before the matched npn output transistors ($Q_3$ & $Q_4$)

The transistors $Q_1$ and $Q_3$ form a darlington connection that provides o/p from a low impedance emitter follower

The connection of transistor $Q_2$ & $Q_4$ forms a feedback pair which similarly provides a low impedance drive to the load. Resistor $R_2$ can be adjusted to minimize crossover distortion by adjusting the dc bias condition.

At point 1 ($\omega t = 0$)

$$i_c = I_{c(max)} = I_{CQ} + I_0 + I_1 \cos 0 + I_2 \cos 2\times 0 + \cdots$$

$$I_{c(max)} = I_{CQ} + I_0 + I_1 + I_2 \quad \rightarrow (1)$$

At point 2 ($\omega t = \pi/2$)

$$I_{CQ} = I_{CQ} + I_0 + I_1 \cos \pi/2 + I_2 \cos 2\pi/2$$

$$I_0 = I_2$$

$$I_c = I_{CQ} = I_{CQ} + I_0 - I_2 \quad \rightarrow (2)$$

At point 3 ($\omega t = \pi$)

$$I_C = I_{c(min)} = I_{CQ} + I_0 + I_1 \cos \pi + I_2 \cos 2\pi$$

$$I_{c(min)} = I_{CQ} + I_0 - I_1 + I_2 \quad \rightarrow (3)$$

Solving for $I_1, I_2, I_0$

Substract (1) - (3)

$$I_{c(max)} - I_{c(min)} = 2I_1$$

$$\boxed{I_1 = \frac{I_{c(max)} - I_{c(min)}}{2}}$$

Add (1) + (3)

$$I_{c(max)} + I_{c(min)} = 2I_{CQ} + 4I_0$$

$$I_0 = I_2 = \frac{I_{c(max)} + I_{c(min)} - 2I_{CQ}}{4}$$

$$\boxed{I_0 = \frac{I_{c(max)} + I_{c(min)} - 2I_{CQ}}{4}}$$

Equation for second harmonic distortion

$$D_2 = \frac{|I_2|}{|I_1|} \times 100$$

$$D_2 = \left| \frac{1/2\left(I_{C(max)} + I_{C(min)}\right) - I_{CQ}}{I_{C(max)} - I_{C(min)}} \right| \times 100$$

In terms of $V_{CE}$

$$D_2 = \left| \frac{1/2\left(V_{CE(max)} + V_{CE(min)}\right) - V_{CEQ}}{V_{CE(max)} - V_{CE(min)}} \right| \times 100\%$$

Power signal having distortion

When distortion does occur the o/p power calculated for the undistorted signal is no longer correct. When distortion is present the output power delivered to the load resistor $R_C$ due to fundamental component of the distorted signal

$$P_1 = \frac{I_1^2 R_C}{2}$$

The total power due to all the harmonic components of the distorted signal can be calculated using

$$P = \left(I_1^2 + I_2^2 + I_3^2 + \cdots\right) R_C/2$$

The total power can also be expressed in terms of THD

$$P = \left(1 + D_2^2 + D_3^2 + \cdots\right) I_1^2 R_C/2$$

$$\boxed{P = (1 + THD^2) P_1}$$

→ A class B power amplifier provides a 20V peak signal to a 16Ω load and a power supply of $V_{CC}=30V$. determine i/p power and o/p power and efficiency

$V_{CC}=30V$

$R_L=16\Omega$

$V_{L(p)}=20V$

$P_{i(dc)} = V_{CC} \cdot I_{CQ}$

$= V_{CC} \cdot \frac{2 \cdot I_{C(p)}}{\pi}$

$= V_{CC} \cdot \frac{2 \times V_{L(p)}}{\pi R_L}$

$= 30 \times 2 \times \frac{20}{\pi \times 16\Omega}$

$I_{C(p)} = I_{L(p)} = \frac{V_{L(p)}}{R_L}$

$= \frac{20}{16}$

$I_{L(p)} = 1.25A$

$$\boxed{P_{i(dc)} = 23.87W}$$

$$P_{o(ac)} = \frac{V_{L(p)}^2}{2R_L} = \frac{20^2}{2 \times 16} = 12.5W$$

$$\eta = \frac{P_{o(ac)}}{P_{i(dc)}} = \frac{12.5W}{23.87W} = 52.3\%$$

→ For class B amplifier using a supply $V_{CC}=30V$ and driving a load of 16Ω determine its maximum i/p power and output power and transistor dissipation.

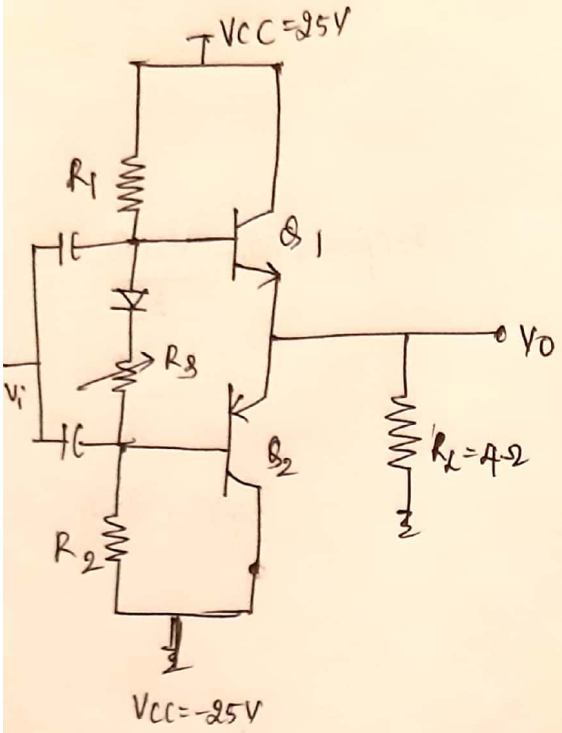
Maximum o/p power is : $P_{o(ac)} = \frac{V_{CC}^2}{2R_L} = \frac{30^2}{2 \times 16\Omega} = 28.125W$

$$P_{i(dc)} = \frac{2V_{CC}^2}{\pi R_L} = \frac{2 \times 30^2}{\pi \times R_L} = 35.81W$$

$$\eta = \frac{28.125}{35.81} = 78.54\%$$

$$P_Q = \frac{1}{2}\left(\frac{2V_{CC}^2}{\pi R_L}\right) = 5.7W$$

→ Calculate i/p power, o/p power and power handled by each output transistor and ckt efficiency for an i/p of 12 V(rms)




$V_{i(p)} = V_{i(rms)} \times \sqrt{2} = 12 \times \sqrt{2} = 16.97 \simeq 17\ V$

W.K.T $V_{(rms)} = \frac{V_{CE(p)}}{\sqrt{2}}$

$\boxed{V_{L(p)} = 17\ V}$

$P_{o(ac)} = \frac{V_{L(p)}^2}{2R_L} = \frac{17^2}{2 \times 4} = 36.125\ W$

$P_{i(dc)} = V_{cc} \cdot I_{CQ}$

$= V_{cc} \cdot \frac{2}{\pi} I_{L(p)}$

$I_{L(p)} = \frac{V_{L(p)}}{R_L} = \frac{17}{4}$

$I_{L(p)} = 4.25\ A$

$= \frac{25 \times 2}{\pi} \times 4.25 A$

$\boxed{P_{i(dc)} = 67.64\ W}$

$\eta = \frac{36.125\ W}{67.64\ W} = 53.3\%$

→ For the above same circuit calculate max-$P_{i(dc)}$ & max $(P_{o(ac)})$ & $\eta$

$P_{o(ac)} = \frac{V_{cc}^2}{2R_L} = \frac{25^2}{2 \times 4} = 78.125\ W$

$P_{i(dc)} = \frac{2V_{cc}^2}{\pi R_L} = \frac{2 \times 25^2}{\pi \times 4} = 99.47\ W$

$\eta = \frac{78.125\ W}{99.47\ W} = 78.54\%$

$P_{2Q} = P_i - P_o = 21.3\ W$

Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5V, second harmonic amplitude of 0.25V, third harmonic of 0.1V and fourth harmonic amplitude of 0.05V & Calculate THD with $R_C = 4\Omega$ & $I_1 = 3.3\,A$

Calculate $P_1$ & $P_T$

$$\%\, D_2 = \frac{|A_2|}{|A_1|} \times 100 = \frac{0.25V}{2.5V} \times 100 = 10\%.$$

$$\%\, D_3 = \frac{|A_3|}{|A_1|} \times 100 = \frac{0.1V}{2.5V} \times 100 = 4\%.$$

$$\%\, D_4 = \frac{|A_4|}{|A_1|} \times 100 = \frac{0.05\,V}{2.5V} \times 100 = 2\%.$$

$$THD = \sqrt{D_2^2 + D_3^2 + D_4^2} \times 100$$

$$= \sqrt{(0.10)^2 + (0.04)^2 + (0.02)^2} \times 100 = 0.1095 \times 100$$

$$= 10.95\%.$$

$$P_1 = \frac{I_1^2 R_C}{2} = \frac{(3.3)^2 \times 4\Omega}{2} = 21.78\,W$$

$$P_T = (1 + THD^2)\, P_1$$

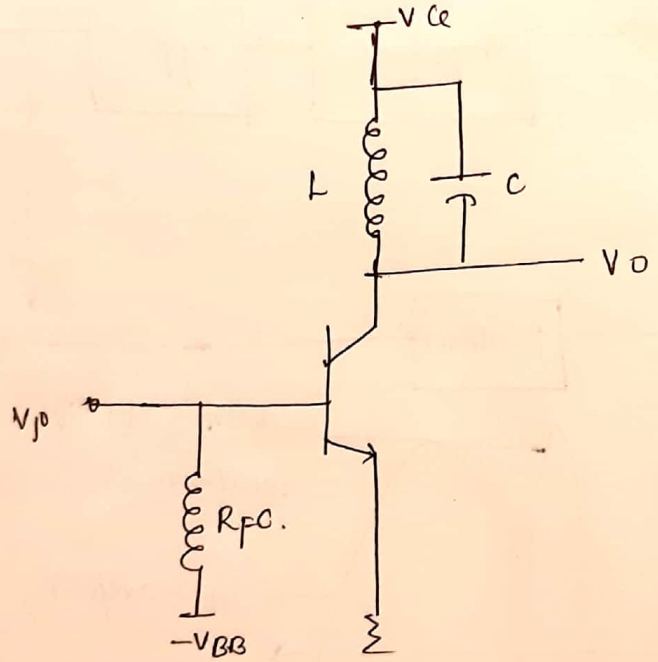
$$\therefore P_T = 22.04\,W \;//.$$

## Class C and class D power Amplifiers

Class C power Amplifiers: Class C PA not used as audio amplifiers do find use in tuned circuits as in Communications.

Class C Amplifiers: Is biased to operate for less than 180° of the input signal cycle. The tuned circuit in the output however will provide a full cycle of output signal for the fundamental or resonant frequency of the tuned circuit. (L and C) tank circuit of the output.

This type of operation is therefore limited to use at one fixed frequency as occurs in a Communication circuits.

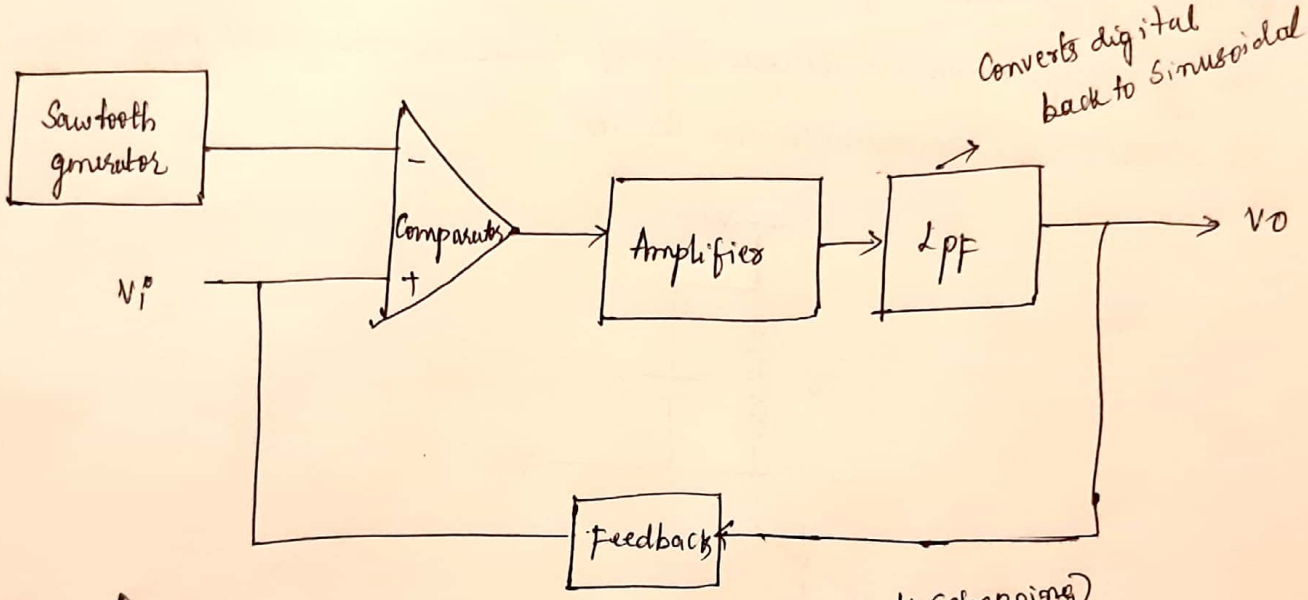


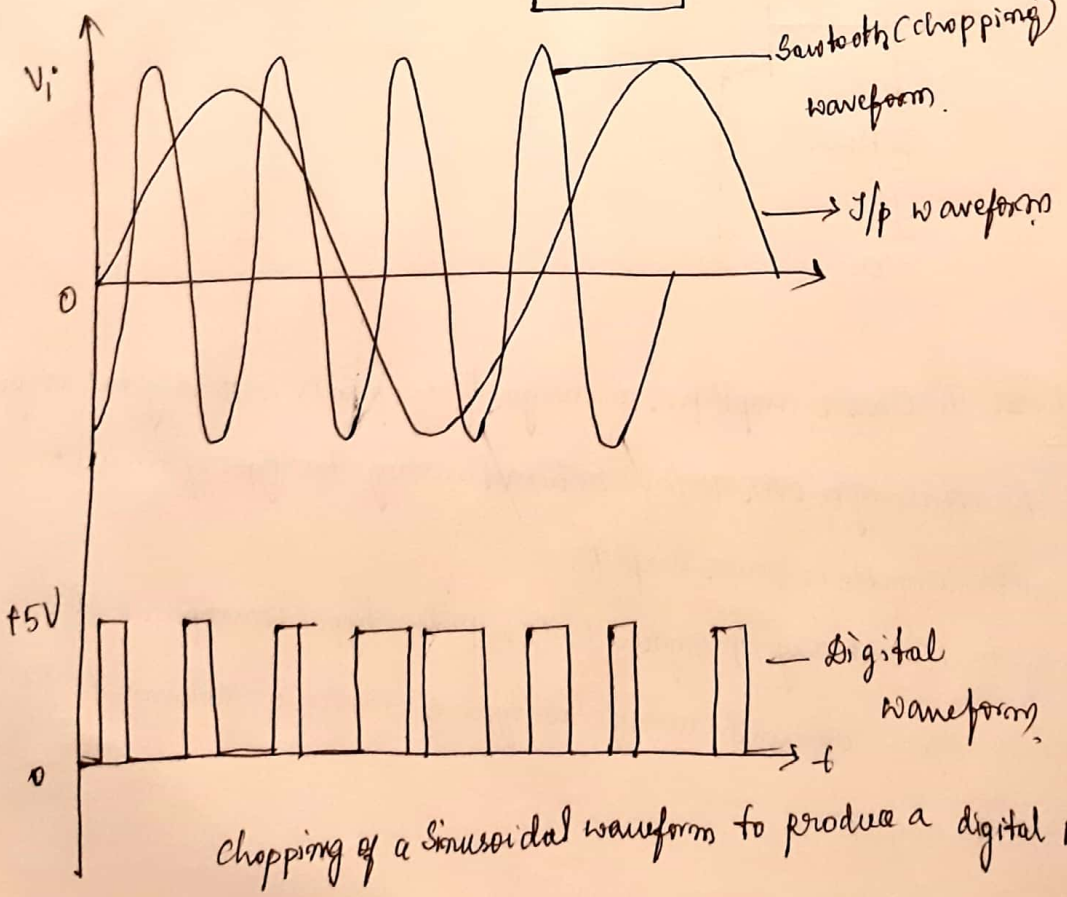

Class D Amplifiers: A class D amplifier is designed to operate with digital or pulse type signals. An efficiency of over 90% is achieved using this type of circuit making it quite desirable in power Amplifiers.

It is necessary to Convert any i/p signal into a pulse type waveform. An efficiency of over 90% is achieved using this type of circuit Making it quite desirable in power amplifiers

To Convert any input Signal into a pulse type waveform before using it to drive a large power load and to Convert the signal back into a Sinusoidal type signal to recover the original Signal.

In the figure below shown the Sinusoidal signal may be applied with the i/p into a Comparator type op-amp CKt so that a representative pulse type Signal is produced.




Chopping of a Sinusoidal waveform to produce a digital waveform.

Block diagram of the unit needed to amplify the class D signal and then convert back into the sinusoidal type signal using a low pass filter since the amplifiers transistor devices used to provide the output are basically either off or on they provide current only when they are turned on with little power loss due to their low on voltage. Since most of the power applied to the amplifier is transferred to the load the efficiency of the circuit is typically very high.

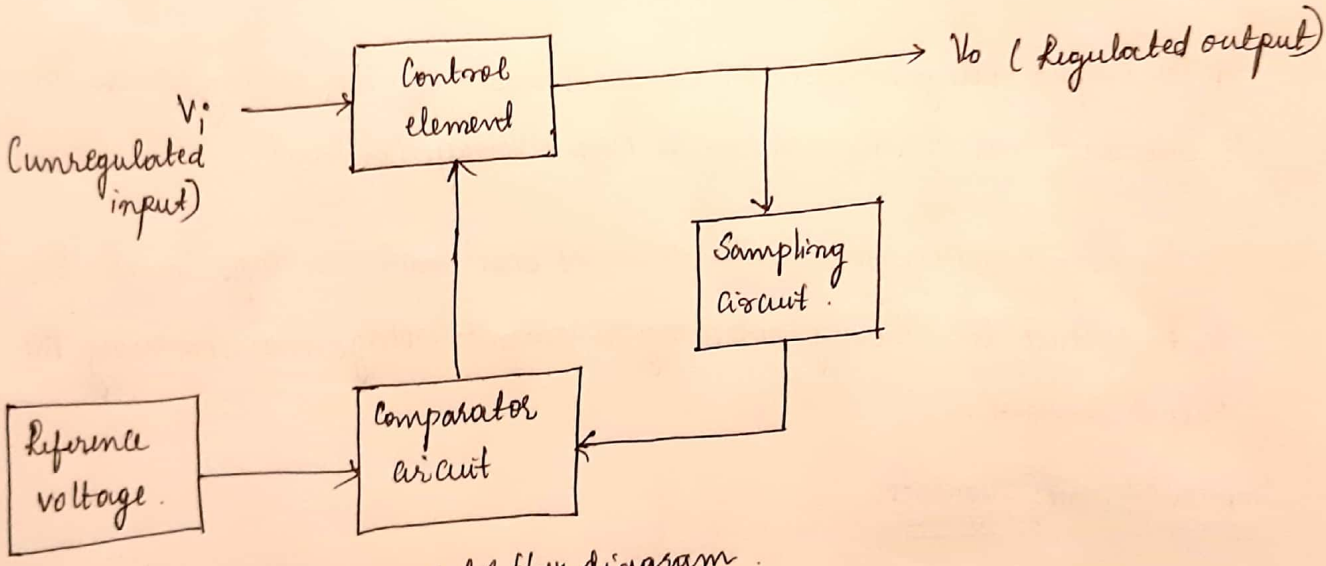
## Discrete transistor voltage Regulation.

Two types of transistor voltage regulators are the Series voltage regulator and the shunt voltage regulator

Each type of circuit can provide an output dc voltage that is regulated or maintained at a set value even if the input voltage varies or if the load connected to the output changes.

### Series voltage Regulation

The basic connection of a Series regulator circuit is shown in the block diagram below The Series element controls the amount of the input voltage that gets to the output




Series regulator block diagram.

The output voltage sampled by a circuit that provides a feedback voltage to be compared to a reference voltage

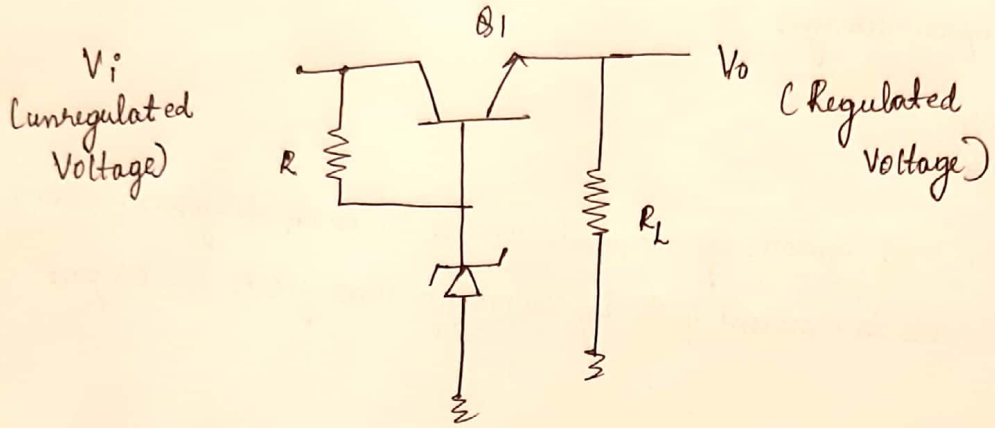
① If the output voltage increases the Comparator circuit provides a Control signal to cause the Series Control element to decrease the amount of the output voltage by maintaing the output voltage.

② If the output voltage decreases the Comparator Cicuit provides a Control Signal to cause the Series Control element to increase the amount of the o/p voltage

Series regulator circuit: A simple series regulator circuit shown below

Transistor $Q_1$ is the series control element and Zener diode $D_Z$ provides the reference voltage.

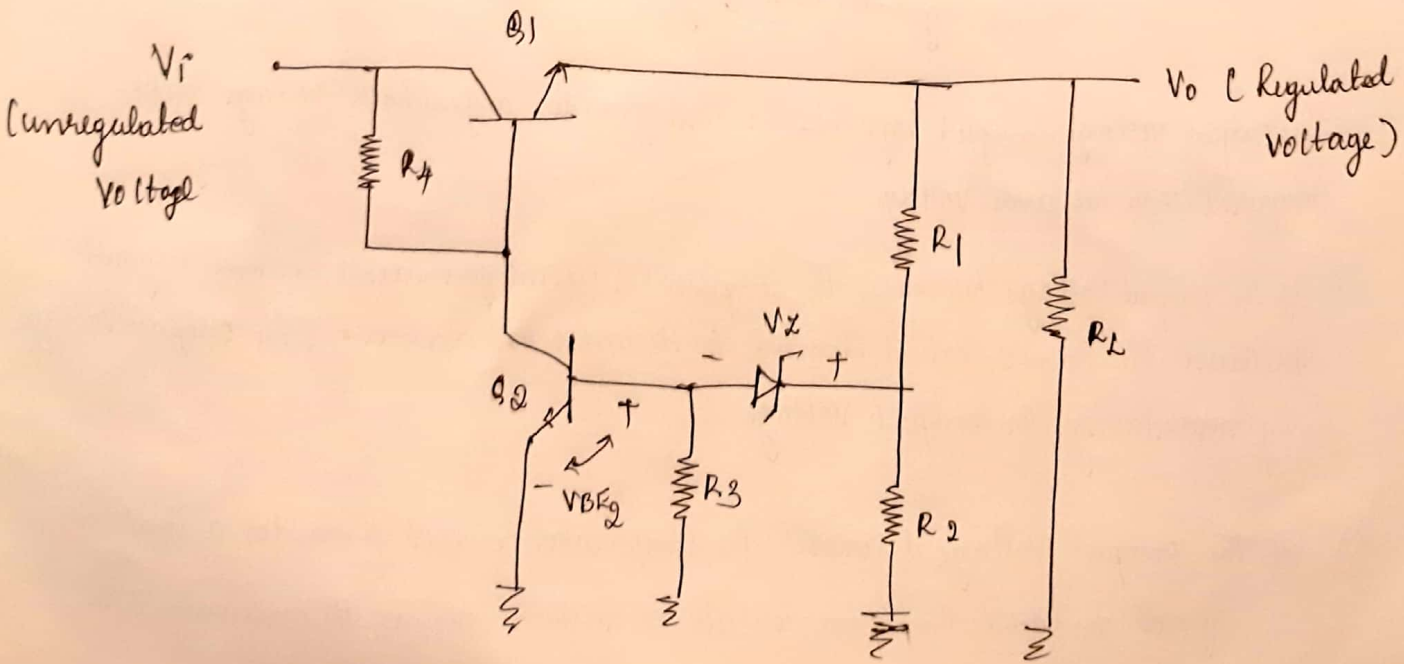
The regulating operation can be described as follows




1. If the output voltage decreases the increased base-emitter voltage causes transistor $Q_1$ to conduct more thereby raising the output voltage constant

2. If the output voltage increases the decreased base-emitter voltage causes transistor $Q_1$ to conduct less, thereby reducing the output voltage maintaining the output constant.

Improved Series regulator



$R_1$ and $R_2$ act as a Sampling circuit with Zener diode $D_Z$ providing a reference voltage and transistor $Q_2$ passes Controls the base current to transistor $Q_1$ to Vary the current passed by transistor $Q_1$ to maintain the output voltage constant.

If the output voltage tries to increase the increased voltage sampled by $R_1$ & $R_2$ increased voltage $V_2$ causes the base emitter voltage of transistor $Q_2$ to go up.

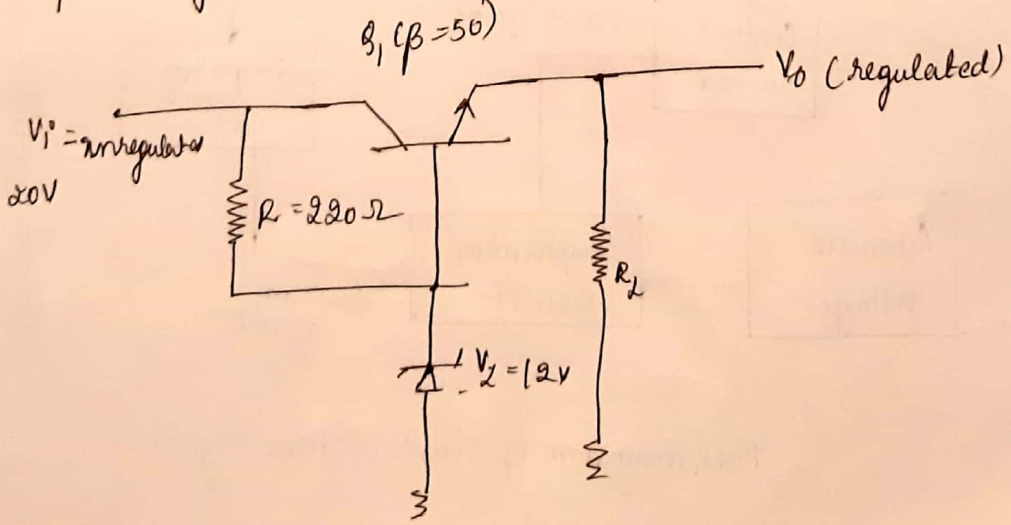
If $Q_2$ conducts more current less goes to the base of the transistor $Q_1$ which then passes less less current to the load reducing the output voltage there by output voltage is maintained constant.

The voltage $V_2$ provided by sensing resistors $R_1$ and $R_2$ must equal the sum of the Base emitter voltage of $Q_2$ and Zener diode that is

$$V_{BE_2} + V_Z = V_2 = \frac{R_2}{R_1 + R_2} V_o$$

$$\boxed{V_o = \frac{R_1 + R_2}{R_2} (V_Z + V_{BE_2})}$$

Calculate the output voltage and Zener current in the regulator circuit with $R_L = 1k\Omega$




$$V_o = V_Z - V_{BE} = 12 - 0.7 = 11.3\ V$$

$V_{CE} = V_i - V_o$

$V_{CE} = 20 - 11.3V = 8.7V$

$$I_R = \frac{V_{cc} - V_z}{R} = \frac{20 - 12}{220\Omega} = 36.4mA$$

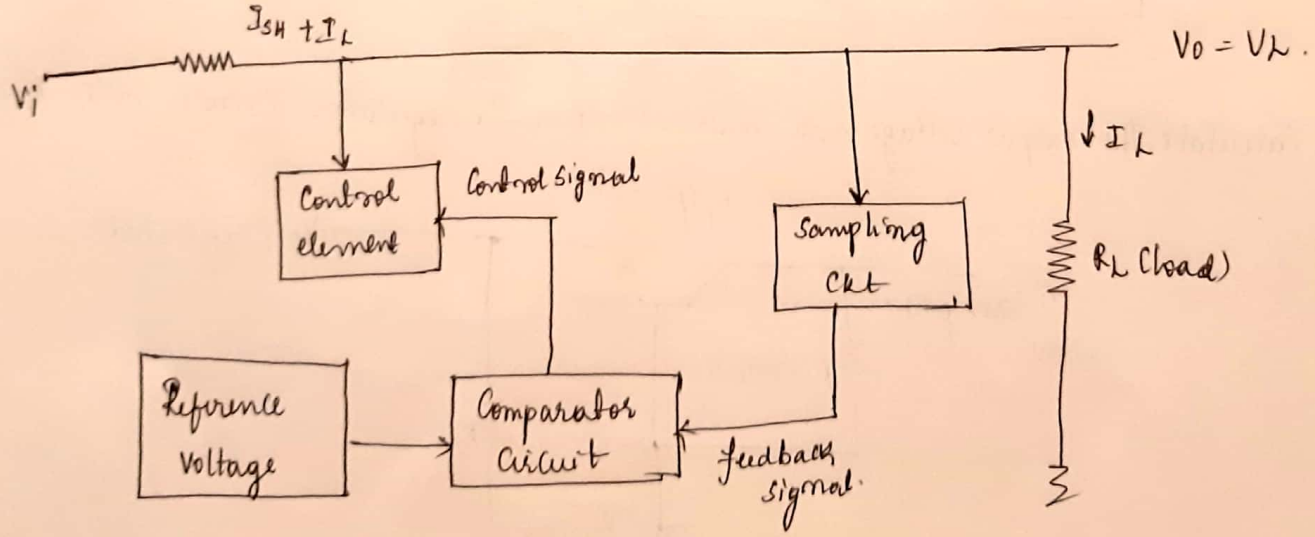
For $R_L = K\Omega$

$$I_C = I_L = \frac{V_o}{R_L} = \frac{11.3V}{1K} = 11.3mA$$

$$I_B = \frac{I_C}{\beta} = \frac{11.3mA}{50} = 226\mu A$$

$$I_Z = I_R - I_B = 36.4mA - 226\mu A = 36mA$$

Shunt voltage regulator : The shunt voltage regulator provides regulation by shunting current away from the load to regulate the o/p voltage figure below shows the block diagram of that

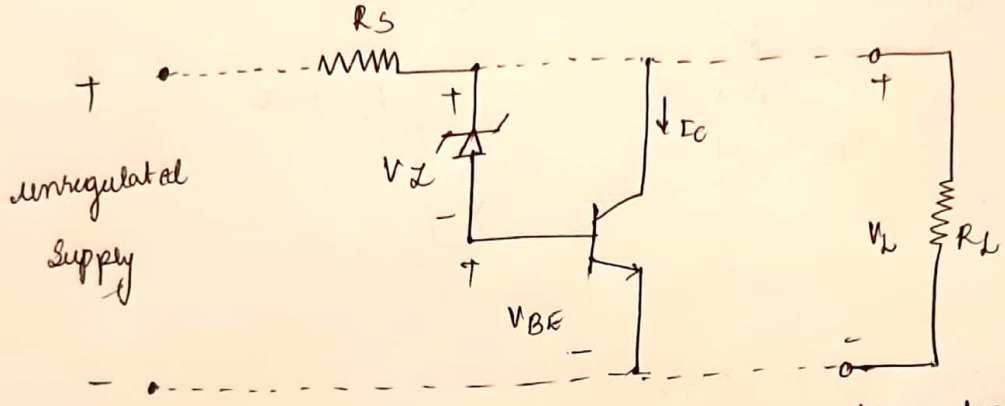



Block diagram of shunt voltage regulator.

The input unregulated voltage provides current to the load. Some of the current is pulled away by the control element to maintain regulated output voltage across the load. If the load voltage tries to change due to change in the load the sampling circuit provides a feedback signal to a comparator. which then provides a control signal to vary the amount of the current shunted away from the load.

As the output voltage tries to get larger

## Basic transistor shunt regulator



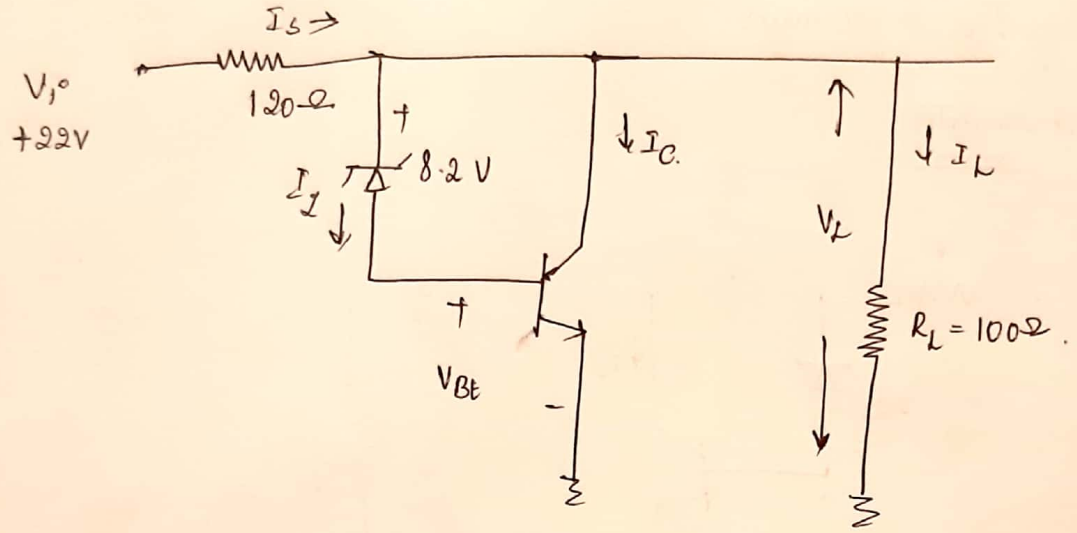

A simple shunt regulator circuit is shown above Resistor $R_S$ drops the unregulated voltage by an amount that depends on the current supplied to the load $R_L$ The voltage across the load is set by the Zener diode and transistor and transistor base emitter voltage. If the load resistance decreases, a reduced drive current to the base of $B_1$ results shunting less collector current. The load current is thus larger. thereby maintaining the regulated voltage across the load. The output voltage to the load is

$$V_L = V_Z + V_{BE}. \quad \rightarrow (1)$$

## Improved Shunt Regulated

The Zener diode provides a reference voltage so that the voltage across $R_1$ senses the output voltage. As the output voltage tries to change the current shunted by transistor $Q_1$ is varied to maintain the output voltage constant. Transistor $Q_2$ provides a larger base current.

→ Determine the regulated voltage and circuit currents for the shunt regulator.




$$V_L = V_Z + V_{BE} = 8.2V + 0.7V = 8.9V$$

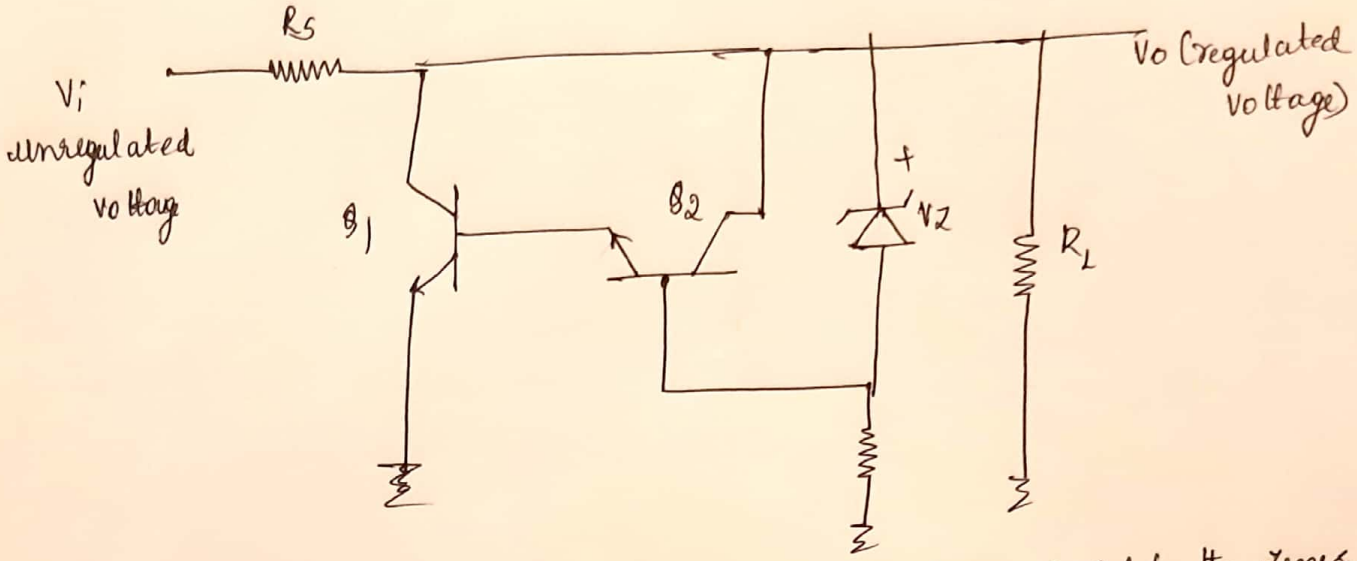
Load current: $I_L = \frac{V_L}{R_L} = \frac{8.9V}{100\Omega} = 89mA$

unregulated i/p at 22V the current through $R_S$ is

$$I_S = \frac{V_i - V_L}{R_S} = \frac{22V - 8.9V}{120\Omega} = 109mA$$

Collector current is $I_C = I_S - I_L = 109mA - 89mA = 20mA$

Improved Shunt Regulator: The Zener diode provides a reference voltage so that the voltage across $R_1$ senses the o/p voltage. As the output voltage tries to change the current shunted by transistor $Q_1$ is varied to maintain the o/p Vtg constant. Transistor $Q_2$ provides a larger base current to transistor $Q_1$




So that the regulator handles a larger load current. The o/p Vtg is set by the Zener voltage and that across the two transistor base-emitters.

$$V_o = V_L = V_Z + V_{BE_1} + V_{BE_2}$$